Dual Input Network Clock Generator/Synchronizer

AD9549

FEATURES

Flexible reference inputs
Input frequencies: 8 kHz to 750 MHz
Two reference inputs
Loss of reference indicators
Auto and manual holdover modes
Auto and manual switchover modes
Smooth A-to-B phase transition on outputs
Excellent stability in holdover mode
Programmable 16 + 1-bit input divider, R
Differential HSTL clock output
Output frequencies to 750 MHz
Low jitter clock doubler for frequencies > 400 MHz
Single-ended CMOS output for frequencies < 150 MHz
Programmable digital loop filter (< 1 Hz to ~100 kHz)
High speed digitally controlled oscillator (DCO) core
DDS with integrated 14-bit DAC
Excellent dynamic performance
Programmable 16 + 1-bit feedback divider, S
Software controlled power-down
64-lead LFCSP package

APPLICATIONS

Network synchronization
Reference clock jitter cleanup
SONET/SDH clocks up to OC-192, including FEC
Stratum 3/3E reference clocks
Wireless base stations, controllers
Cable infrastructure
Data communications

GENERAL DESCRIPTION

The AD9549 provides synchronization for many systems, including synchronous optical networks (SONET/SDH). The AD9549 generates an output clock, synchronized to one of two external input references. The external references may contain significant time jitter, also specified as phase noise. Using a digitally controlled loop and holdover circuitry, the AD9549 continues to generate a clean (low jitter), valid output clock during a loss of reference condition, even when both references have failed.

The AD9549 operates over an industrial temperature range of −40°C to +85°C.

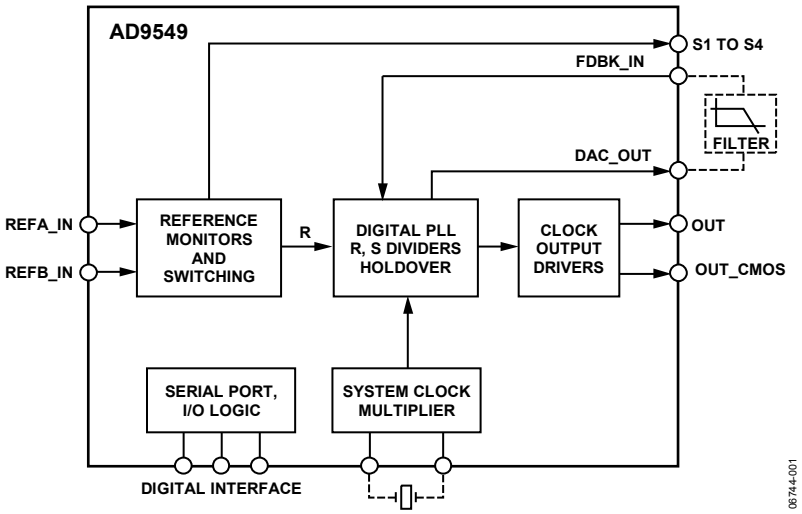

Figure 1. Basic Block Diagram

Rev. 0

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REVISION HISTORY

8/07—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

Unless otherwise noted, AVDD = 1.8 V ± 5%, AVDD3 = 3.3 V ± 5%, DVDD = 1.8 V ± 5%, DVDD_I/O = 3.3 V ± 5%. AVSS = 0 V, DVSS = 0 V.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE					
DVDD_I/O (Pin 1)	3.135	3.30	3.465	V	
DVDD (Pin 3, Pin 5, Pin 7)	1.71	1.80	1.89	V	
AVDD3 (Pin 14, Pin 46, Pin 47, Pin 49)	3.135	3.30	3.465	V	
AVDD3 (Pin 37)	1.71	3.30	3.465	V	Pin 37 is typically 3.3 V, but can be set to 1.8 V
AVDD (Pin 11, Pin 19, Pin 23 to Pin 26, Pin 29, Pin 30, Pin 36, Pin 42, Pin 44, Pin 45, Pin 53)	1.71	1.80	1.89	V	
SUPPLY CURRENT					
I_{AVDD3} (Pin 14)		4.7	5.6	mA	REFA, REFB buffers
I_{AVDD3} (Pin 37)		3.8	4.5	mA	CMOS output clock driver at 3.3 V
I_{AVDD3} (Pin 46, Pin 47, Pin 49)		26	29	mA	DAC output current source, f_S = 1 GSPS
I_{AVDD} (Pin 36, Pin 42)		21	26	mA	FDBK in, HSTL output clock driver (output doubler turned on.)
I_{AVDD} (Pin 11)		12	15	mA	REFA and REFB input buffer 1.8 V supply
I_{AVDD} (Pin 19, Pin 23 to Pin 26, Pin 29, Pin 30, Pin 44, Pin 45)		194	255	mA	Aggregate analog supply, including system clock PLL
I_{AVDD} (Pin 53)		41	49	mA	DAC power supply
I_{DVDD} (Pin 3, Pin 5, Pin 7)		254	265	mA	Digital core
$I_{DVDD\_I/O}$ (Pin 1)		4	6	mA	Digital I/O (varies dynamically)
LOGIC INPUTS (Except Pin 32)					Pin 56 to Pin 61, Pin 64, Pin 9, Pin 10, Pin 54, Pin 55, Pin 63
Input High Voltage (V_{IH})	2.0		DVDD_I/O	V	
Input Low Voltage (V_{IL})	DVSS		0.8	V	
Input Current (I_{INH}, I_{INL})		±60	±200	µA	At V_{IN} = 0 V and V_{IN} = DVDD_I/O
Maximum Input Capacitance (C_{IN})		3		pF	
CLKMODESEL (Pin 32) LOGIC INPUT					Pin 32 only
Input High Voltage (V_{IH})	1.4		AVDD	V	
Input Low Voltage (V_{IL})	AVSS		0.4	V	
Input Current (I_{INH}, I_{INL})		−18	−50	µA	At V_{IN} = 0 V and V_{IN} = AVDD
Maximum Input Capacitance (C_{IN})		3		pF	
LOGIC OUTPUTS					Pin 62 and bidirectional Pin 9, Pin 10, Pin 54, Pin 55, and Pin 63
Output High Voltage (V_{OH})	2.7		DVDD	V	I_{OH} = 1 mA
Output Low Voltage (V_{OL})	DVSS		0.4	V	I_{OL} = 1 mA
REFERENCE INPUTS					Pin 12, Pin 13, Pin 15, Pin 16
Input Capacitance		3		pF	
Input Resistance	8.5	11.5	14.5	kΩ	Differential at Register 40F[1:0] = 00
Differential Operation					
Common Mode Input Voltage[1] (Applicable When DC-Coupled)	1.5		AVDD3 – 0.2	V	Differential operation; note that LVDS signals must be ac-coupled
Differential Input Voltage Swing[1]	500			mV p-p	Differential operation
Single-Ended Operation					Register 040F[1:0] = 10
Input Voltage High (V_{IH})	2.0		AVDD3	V	
Input Voltage Low (V_{IL})	AVSS		0.8	V	
Threshold Voltage	AVDD3 – 0.66	AVDD3 – 0.82	AVDD3 – 0.98	V	Register 040F[1:0] = 10 (other settings possible)
Input Current			1	mA	Single-ended operation

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FDBK INPUT					Pin 40, Pin 41
Input Capacitance		3		pF	
Input Resistance	18	22	26	kΩ	Differential
Differential Input Voltage Swing[2]	225			mV p-p	−12 dBm into 50 Ω; must be ac-coupled
SYSTEM CLOCK INPUT					System clock inputs should always be ac-coupled (both single-ended and differential)
SYSCLK PLL Bypassed					
Input Capacitance		1.5		pF	Single-ended, each pin
Input Resistance	2.4	2.6	2.8	kΩ	Differential
Internally Generated DC Bias Voltage[2]	0.93	1.17	1.38	V	
Differential Input Voltage Swing[3]	632			mV p-p	0 dBm into 50 Ω
SYSCLK PLL Enabled					
Input Capacitance		3		pF	Single-ended, each pin
Input Resistance	2.4	2.6	2.8	kΩ	Differential
Internally Generated DC Bias Voltage[2]	0.93	1.17	1.38	V	
Differential Input Voltage Swing[3]	632			mV p-p	0 dBm into 50 Ω
Crystal Resonator with SYSCLK PLL Enabled					
Motional Resistance		9	100	Ω	25 MHz, 3.2 mm × 2.5 mm AT cut
CLOCK OUTPUT DRIVERS					
HSTL Output Driver					
Differential Output Voltage Swing	1080	1280	1480	mV	Output driver static, see Figure 12 for output swing vs. frequency
Common-Mode Output Voltage[2]	0.7	0.88	1.06	V	
CMOS Output Driver					Output driver static, see Figure 14 for output swing vs. frequency
Output Voltage High (V_{OH}) AVDDX = 3.3 V	2.7			V	I_{OH} = 1 mA.
Output Voltage Low (V_{OL}) AVDDX = 3.3 V			0.4	V	I_{OL} = 1 mA.
Output Voltage High (V_{OH}) AVDDX = 1.8 V	1.4			V	I_{OH} = 1 mA.
Output Voltage Low (V_{OL}) AVDDX = 1.8 V			0.4	V	I_{OL} = 1 mA.
TOTAL POWER DISSIPATION					
All Blocks Running		1010	1250	mW	Worst case over supply, temperature, process
Power-Down Mode		24		mW	Using either the Power-Down and Enable register or PWRDOWN pin
Digital Power-Down Mode		515	650	mW	
Default with SYSCLK PLL Enabled		905	1100	mW	After reset or power up with f_S = 1 GHz, S4 = 0, S1 to S3 = 1, f_{SYSCLK} = 25MHz
Default with SYSCLK PLL Disabled		895	1056	mW	After reset or power up with f_S = 1 GHz, S1 to S4 = 1
With REFA or REFB Power-Down			1046	mW	One reference still powered up
With HSTL Clock Driver Power-Down			1036	mW	
With CMOS Clock Driver Power-Down			1048	mW	

[1] Must be ≤ 0 V relative to AVDD3 (Pin 14) and ≥ 0 V relative to AVSS (Pin 33, Pin 43).
[2] Relative to AVSS (Pin 33, Pin 43).
[3] Must be ≤ 0 V relative to AVDD (Pin 36) and ≥ 0 V relative to AVSS (Pin 33, Pin 43).

AC SPECIFICATIONS

Unless otherwise noted, f_S = 1 GHz. DAC R_{SET} = 10 kΩ. Power supply pins within the range specified in the DC Specifications section.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE INPUTS					Pin 12, Pin 13, Pin 15, Pin 16
Frequency Range (Sine Wave)	10		750	MHz	Minimum recommended slew rate: 40 V/µs
Frequency Range (CMOS)	0.008		50	MHz	
Frequency Range (LVPECL)	0.008		725	MHz	
Frequency Range (LVDS)	0.008		725	MHz	LVDS must be ac-coupled; lower frequency bound may be higher depending on size of decoupling capacitor
Minimum Slew Rate	0.04			V/ns	
Minimum Pulse Width High	620			ps	
Minimum Pulse Width Low	620			ps	
FDBK INPUT					Pin 40, Pin 41
Input Frequency Range	10		400	MHz	
Minimum Differential Input Level	225			mV p-p	−12 dBm into 50 Ω; must be ac-coupled
Minimum Slew Rate	40			V/µs	
SYSTEM CLOCK INPUT					Pin 27, Pin 28
SYSCLK PLL Bypassed					
Input Frequency Range	250		1000	MHz	Maximum f_{OUT} is 0.4 × f_{SYSCLK}
Duty Cycle	45		55	%	
Minimum Differential Input Level	632			mV p-p	0 dBm into 50 Ω
SYSCLK PLL Enabled					
VCO Frequency Range, Low Band	700		810	MHz	When in the range, use the low VCO band exclusively
VCO Frequency Range, Auto Band	810		900	MHz	When in the range, use the VCO Auto band select
VCO Frequency Range, High Band	900		1000	MHz	When in the range, use the high VCO band exclusively
Maximum Input Rate of System Clock PFD			100	MHz	
Without SYSCLK PLL Doubler					
Input Frequency Range	11		200	MHz	
Multiplication Range	4		66		Integer multiples of 2, maximum PFD rate and system clock frequency must be met
Minimum Differential Input Level	632			mV p-p	0 dBm into 50 Ω
With SYSCLK PLL Doubler					
Input Frequency Range	6		100	MHz	
Multiplication Range	8		132		Integer multiples of 8
Input Duty Cycle		50		%	Deviating from 50% duty cycle may adversely affect spurious performance.
Minimum Differential Input Level	632			mV p-p	0 dBm into 50 Ω
Crystal Resonator with SYSCLK PLL Enabled					
Crystal Resonator Frequency Range	10		50	MHz	AT cut, fundamental mode resonator
Maximum Crystal Motional Resistance			100	Ω	See the SYSCLK Inputs section for recommendations
CLOCK DRIVERS					
HSTL Output Driver					
Frequency Range	20		725	MHz	See Figure 12 for maximum toggle rate
Duty Cycle	48		52	%	
Rise/Fall Time (20-80%)		115	165	ps	100 Ω termination across OUT/OUTB, 2 pF load
Jitter (12 kHz to 20 MHz)		1.0		ps	f_{IN} = 19.44 MHz, f_{OUT} = 155.52 MHz. 50 MHz system clock input (see Figure 3 to Figure 11 for test conditions)
HSTL Output Driver with 2× Multiplier					
Frequency Range	400		725	MHz	
Duty Cycle	45		55	%	
Rise/Fall Time (20% to 80%)		115	165	ps	100 Ω termination across OUT/OUTB, 2 pF load
Sub-harmonic Spur Level		−35		dBc	Without correction
Jitter (12 kHz to 20 MHz)		1.1		ps	f_{IN} = 19.44 MHz, f_{OUT} = 622.08 MHz, 50 MHz system clock input (see Figure 3 to Figure 11 for test conditions)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CMOS Output Driver (AVDD3/Pin 37) @ 3.3 V					
Frequency Range	0.008		150	MHz	See Figure 14 for maximum toggle rate
Duty Cycle	45	55	65	%	With 20 pF load and up to 150 MHz
Rise/Fall Time (20-80%)		3	4.6	ns	With 20 pF load
CMOS Output Driver (AVDD3/Pin 37) @ 1.8 V					
Frequency Range	0.008		40	MHz	See Figure 13 for maximum toggle rate
Duty Cycle	45	55	65	%	With 20 pF load and up to 40 MHz
Rise/Fall Time (20% to 80%)		5	6.8	ns	With 20 pF load
HOLDOVER					
Frequency Accuracy					See the Holdover section
OUTPUT FREQUENCY SLEW LIMITER					
Slew Rate Resolution	0.54		111	Hz/sec	$P = 2^{16}$ for minimum; $P = 2^5$ for maximum
Slew Rate Range	0		3×10^{16}	Hz/sec	$P = 2^{16}$ for minimum; $P = 2^5$ for maximum
REFERENCE MONITORS					
Loss of Reference Monitor					
Operating Frequency Range	7.63×10^3		167×10^6	Hz	
Minimum Frequency Error for Continuous REF Present Indication			−16	ppm	f_{REF} = 8 kHz
Minimum Frequency Error for Continuous REF Present Indication			−19	%	f_{REF} = 155 MHz
Maximum Frequency Error for Continuous REF Lost Indication	−32			ppm	f_{REF} = 8 kHz
Maximum Frequency Error for Continuous REF Lost Indication	−35			%	f_{REF} = 155 MHz
Reference Quality Monitor					
Operating Frequency Range	0.008		150	MHz	
Frequency Resolution (Normalized)	0.2			ppm	f_{REF} = 8 kHz; OOL divider = 65,535 for minimum; OOL divider = 1 for max (see the Reference Frequency Monitor section)
Frequency Resolution (Normalized)	408			ppm	f_{REF} = 155 MHz; OOL divider = 65,535 for minimum; OOL divider = 1 for maximum
Validation Timer					See the Reference Validation Timers section
Timing Range	32×10^{-9}		137	s	P_{IO} = 5
Timing Range	65×10^{-6}		2.8×10^5	s	P_{IO} = 16
DAC OUTPUT CHARACTERISTICS					
DCO Frequency Range (1st Nyquist Zone)	10		450	MHz	DPLL loop bandwidth sets lower limit
Output Resistance		50		Ω	Single-ended (each pin internally terminated to AVSS)
Output Capacitance		5		pF	
Full-Scale Output Current		20	31.7	mA	Range depends on DAC R_{SET} resistor
Gain Error	−10		+10	%FS	
Output Offset			0.6	µA	
Voltage Compliance Range	AVSS − 0.50	+0.5	AVSS + 0.50		Outputs not dc-shorted to V_{SS}
DIGITAL PLL					
Minimum Open-Loop Bandwidth		0.1		Hz	Dependent on the frequency of REFA/REFB, the DAC sample rate, and the P-, R-, and S-divider values
Maximum Open-Loop Bandwidth		100		kHz	Dependent on the frequency of REFA/REFB, the DAC sample rate, and the P-, R-, and S-divider values
Minimum Phase Margin	0	10		Degrees	Dependent on the frequency of REFA/REFB, the DAC sample rate, and the P-, R-, and S-divider values
Maximum Phase Margin		85	90	Degrees	Dependent on the frequency of REFA/REFB, the DAC sample rate, and the P-, R-, and S-divider values
PFD Input Frequency Range	~0.008		~24.5	MHz	
Feedforward Divider Ratio	1		131,070		1, 2, …,65,535 or 2, 4, …, 131,070
Feedback Divider Ratio	1		131,070		1, 2, …, 65,535 or 2, 4, …, 131,070

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOCK DETECTION					
Phase Lock Detector					
Time Threshold Programming Range	0		2097	µs	FPFD_Gain = 200
Time Threshold Resolution		0.488		ps	FPFD_Gain = 200
Lock Time Programming Range	32×10^{-9}		275	s	In power-of-2 steps
Unlock Time Programming Range	192×10^{-9}		67×10^{-3}	s	In power-of-2 steps
Frequency Lock Detector					
Normalized Frequency Threshold Programming Range	0		0.0021		FPFD_Gain = 200; normalized to $(f_{REF}/R)^2$; see the Frequency Lock Detection section for details
Normalized Frequency Threshold Programming Resolution		5×10^{-13}			FPFD_Gain = 200; normalized to $(f_{REF}/R)^2$; see the Frequency Lock Detection section for details
Lock Time Programming Range	32×10^{-9}		275	s	In power-of-2 steps
Unlock Time Programming Range	192×10^{-9}		67×10^{-3}	s	In power-of-2 steps
DIGITAL TIMING SPECIFICATIONS					
Time Required to Enter Power-Down		15		µs	
Time Required to Leave Power-Down		18		µs	
Reset Assert to High-Z Time for S1 to S4 Configuration Pins		60		ns	Time from rising edge of RESET to high-Z on the S1, S2, S3, S4 configuration pins
Reset Deassert to Low-Z Time for S1 to S4 Configuration Pins		30		ns	Time from falling edge of RESET to low-Z on the S1, S2, S3, S4 configuration pins
SERIAL PORT TIMING SPECIFICATIONS					
SCLK Clock Rate ($1/t_{CLK}$)		25	50	MHz	Refer to Figure 58 for all write-related serial port parameters, maximum SCLK rate for readback is governed by t_{DV}
SCLK Pulse Width High, t_{HI}	8			ns	
SCLK Pulse Width Low, t_{LO}	8			ns	
SDO/SDIO to SCLK Setup Time, t_{DS}	1.93			ns	
SDO/SDIO to SCLK Hold Time, t_{DH}	1.9			ns	
SCLK Falling Edge to Valid Data on SDIO/SDO, t_{DV}			11	ns	Refer to Figure 56
CSB to SCLK Setup Time, t_S	1.34			ns	
CSB to SCLK Hold Time, t_H	−0.4			ns	
CSB Minimum Pulse Width High, t_{PWH}	3			ns	
PROPAGATION DELAY					
FDBK to HSTL Output Driver		2.8		ns	
FDBK to HSTL Output Driver with 2× Frequency Multiplier Enabled		7.3		ns	
FDBK to CMOS Output Driver		8.0		ns	
FDBK Through S-Divider to CMOS Output Driver		8.6		ns	

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Analog Supply Voltage (AVDD)	2 V
Digital Supply Voltage (DVDD)	2 V
Digital I/O Supply Voltage (DVDD_I/O)	3.6 V
DAC Supply Voltage (DAC_VDD)	3.6 V
Maximum Digital Input Voltage	−0.5 V to DVDD_I/O + 0.5 V
Storage Temperature	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C
Thermal Resistance[1]	
θ_{JA}	25.2°C/W typical
θ_{JB}	13.9°C/W typical
θ_{JC}	1.7°C/W typical

[1] The exposed pad on bottom of package must be soldered to ground in order to achieve the specified thermal performance. See the Thermal Performance section for more information.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

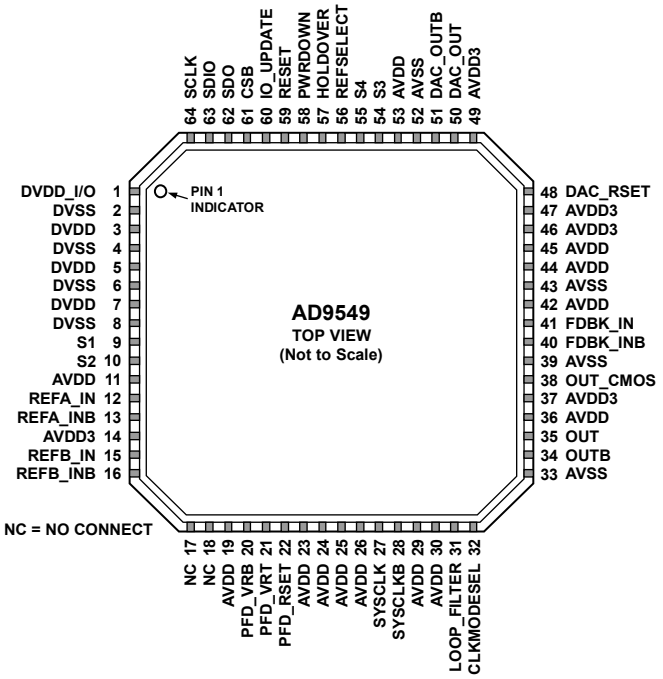


Figure 2. 64-Lead LFCSP Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Input/ Output	Pin Type	Mnemonic	Description
1	I	Power	DVDD_I/O	I/O Digital Supply.
2, 4, 6, 8	I	Power	DVSS	Digital Ground. Connect to ground.
3, 5, 7	I	Power	DVDD	Digital Supply.
9, 10, 54, 55	I/O	3.3 V CMOS	S1, S2, S3, S4	Configurable I/O Pins. These pins are configured under program control (see the Status and Warnings section) and do not have internal pull-up/pull-down resistors.
11, 19, 23 to 26, 29, 30, 36, 42, 44, 45, 53	I	Power	AVDD	Analog Supply. Connect to a nominal 1.8 V supply.
12	I	Differential Input	REFA_IN	Frequency/Phase Reference A Input. This internally biased input is typically ac-coupled and, when configured as such, can accept any differential signal with single-ended swing between 0.4 V and 3.3 V. If dc-coupled, LVPECL or CMOS input is preferred.
13	I	Differential Input	REFA_INB	Complementary Frequency/Phase Reference A Input. Complementary signal to the input provided on Pin 12. If using a single-ended, dc-coupled CMOS signal into REFA_IN, bypass this pin to ground with a 0.01 µF capacitor.
14, 46, 47, 49	I	Power	AVDD3	Analog Supply. Connect to a nominal 3.3 V supply.
15	I	Differential Input	REFB_IN	Frequency/Phase Reference B Input. This internally biased input is typically ac-coupled and, when configured as such, can accept any differential signal with single-ended swing between 0.4 V and 3.3 V. If dc-coupled, LVPECL or CMOS input is preferred.
16	I	Differential Input	REFB_INB	Complementary Frequency/Phase Reference B Input. Complementary signal to the input provided on Pin 15. If using a single-ended, dc-coupled CMOS signal into REFB_IN, bypass this pin to ground with a 0.01 µF capacitor.
17, 18			NC	No Connect. These are excess, unused pins that can be left floating.
20, 21	O		PFD_VRB, PFD_VRT	These pins must be capacitively decoupled. See the Phase Detector Pin Connections section for details.

Pin No.	Input/ Output	Pin Type	Mnemonic	Description
22	O	Current Set Resistor	PFD_RSET	Connect a 5 kΩ resistor from this pin to ground (see the Phase Detector Pin Connections section).
27	I	Differential Input	SYSCLK	System Clock Input. The system clock input has internal dc biasing and should always be ac-coupled, except when using a crystal. Single-ended 1.8 V CMOS can also be used but can introduce a spur caused by an input duty cycle that is not 50%. When using a crystal, tie the CLKMODESEL pin to AVSS, and connect crystal directly to this pin and Pin 28.
28	I	Differential Input	SYSCLKB	Complementary System Clock. Complementary signal to the input provided on Pin 27. Use a 0.01 µF capacitor to ground on this pin if the signal provided on Pin 27 is single-ended.
31	O		LOOP_FILTER	System Clock Multiplier Loop Filter. When using the frequency multiplier to drive the system clock, an external loop filter must be constructed and attached to this pin. This pin is pulled high when the system clock PLL is bypassed and can be left floating in this mode. See Figure 44 for a diagram of the system clock PLL loop filter.
32	I	1.8 V CMOS	CLKMODESEL	Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pin 27 and Pin 28). Pull up to 1.8 V when using either an oscillator or an external clock source. This pin can be left floating when the system clock PLL is bypassed. (See the SYSCLK Inputs section for details on the use of this pin.)
33, 39, 43, 52	O	GND	AVSS	Analog Ground. Connect to ground.
34	O	1.8 V HSTL	OUTB	Complementary HSTL Output. See the Specifications and Primary 1.8 V Differential HSTL Driver sections for details.
35	O	1.8 V HSTL	OUT	HSTL Output. See the Specifications and Primary 1.8 V Differential HSTL Driver sections for details.
37	I	Power	AVDD3	Analog Supply for CMOS Output Driver: This pin is normally 3.3 V but can be 1.8 V. This pin should be powered even if the CMOS driver is not used. See the Power Supply Partitioning section for power supply partitioning.
38	O	3.3 V CMOS	OUT_CMOS	CMOS Output. See the Specifications section and the Output Clock Drivers and 2× Frequency Multiplier section. This pin is 1.8 V CMOS if Pin 37 is set to 1.8 V.
40	I	Differential Input	FDBK_INB	Complementary Feedback Input. In standard operating mode, this pin is connected to the filtered DAC_OUTB output. This internally biased input is typically ac-coupled, and when configured as such, can accept any differential signal whose single-ended swing is at least 400 mV.
41	I	Differential Input	FDBK_IN	Feedback Input. In standard operating mode, this pin is connected to the filtered DAC_OUT output
48	O	Current Set Resistor	DAC_RSET	DAC Output Current Setting Resistor. Connect a resistor (usually 10 kΩ) from this pin to GND. See the DAC Output section.
50	O	Differential Output	DAC_OUT	DAC Output. This signal should be filtered and sent back on chip through FDBK_IN input. This pin has an internal 50 Ω pull-down resistor.
51	O	Differential Output	DAC_OUTB	Complimentary DAC Output. This signal should be filtered and sent back on chip through FDBK_INB input. This pin has an internal 50 Ω pull-down resistor.
56	I/O	3.3 V CMOS	REFSELECT	Reference Select Input. In manual mode, the REFSELECT pin operates as a high impedance input pin, while in automatic mode, it operates as a low impedance output pin. Logic 0 (low) indicates/selects REFA. Logic 1 (high) indicates/selects REFB. There is no internal pull-up/pull-down resistor on this pin.
57	I/O	3.3 V CMOS	HOLDOVER	Holdover (Active High). In manual holdover mode, this pin is used to force the AD9549 into holdover mode. In automatic holdover mode, it indicates holdover status. There is no internal pull-up/pull-down resistor on this pin.
58	I	3.3 V CMOS	PWRDOWN	Power-Down. When this active high pin is asserted, the device becomes inactive and enters the full power-down state. This pin has an internal 50 kΩ pull-down resistor.
59	I	3.3 V CMOS	RESET	Chip Reset. When this active high pin is asserted, the chip goes into reset. Note that on power-up, a 10 µs reset pulse is internally generated when the power supplies reach a threshold and stabilize. This pin has an internal 50 kΩ pull-down resistor.
60	I	3.3 V CMOS	IO_UPDATE	I/O Update. A logic transition from 0 to 1 on this pin transfers data from the I/O port registers to the control registers (see the Write section). This pin has an internal 50 kΩ pull-down resistor.

Pin No.	Input/ Output	Pin Type	Mnemonic	Description
61	I	3.3 V CMOS	CSB	Chip Select. Active low. When programming a device, this pin must be held low. In systems where more than one AD9549 is present, this pin enables individual programming of each AD9549. This pin has an internal 100 kΩ pull-up resistor.
62	O	3.3 V CMOS	SDO	Serial Data Output. When the device is in 3-wire mode, data is read on this pin. There is no internal pull-up/pull-down resistor on this pin.
63	I/O	3.3 V CMOS	SDIO	Serial Data Input/Output. When the device is in 3-wire mode, data is written via this pin. In 2-wire mode, data reads and writes both occur on this pin. There is no internal pull-up/pull-down resistor on this pin.
64	I	3.3 V CMOS	SCLK	Serial Programming Clock. Data clock for serial programming. This pin has an internal 50 kΩ pull-down resistor.
Exposed Die Pad	O	GND	AVSS	Analog Ground. Connect to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, AVDD, AVDD3, and DVDD at nominal supply voltage; f_S = 1 GHz, DAC R_{SET} = 10 kΩ.

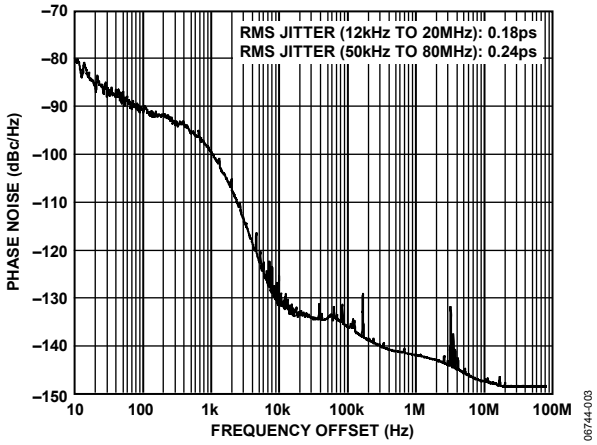


Figure 3. Additive Phase Noise at HSTL Output Driver, SYSCLK = 1 GHz (SYSCLK PLL Bypassed), f_{REF} = 19.44 MHz, f_{OUT} = 311.04 MHz, DPLL Loop BW = 1 kHz

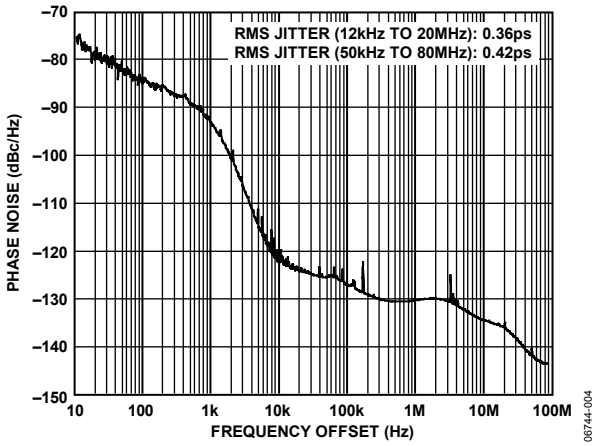


Figure 4. Additive Phase Noise at HSTL Output Driver, SYSCLK = 1 GHz (SYSCLK PLL Bypassed), f_{REF} = 19.44 MHz, f_{OUT} = 622.08 MHz, DPLL Loop BW = 1 kHz, HSTL Output Doubler Enabled

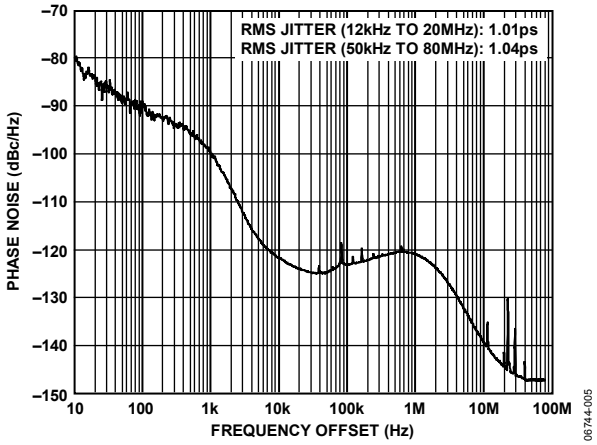


Figure 5. Additive Phase Noise at HSTL Output Driver, SYSCLK = 1 GHz (SYSCLK PLL Enabled Driven by R&S SMA100 Signal Generator at 50 MHz), f_{REF} = 19.44 MHz, f_{OUT} = 311.04 MHz, DPLL Loop BW = 1 kHz

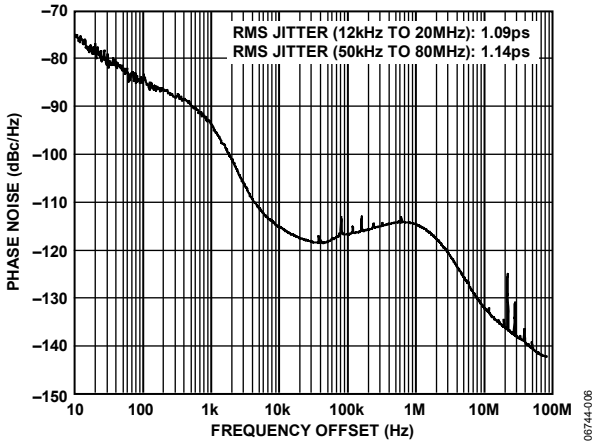


Figure 6. Additive Phase Noise at HSTL Output Driver, SYSCLK = 1 GHz (SYSCLK PLL Enabled and Driven by R&S SMA100 Signal Generator at 50 MHz), f_{REF} = 19.44 MHz, f_{OUT} = 622.08 MHz, DPLL Loop BW = 1 kHz, System Clock Doubler Enabled, HSTL Doubler Enabled

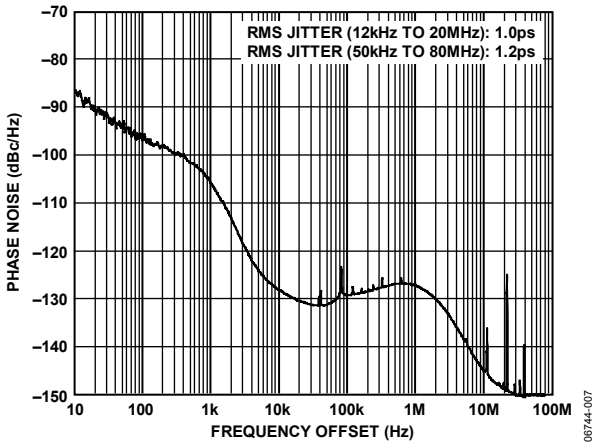


Figure 7. Additive Phase Noise at HSTL Output Driver, SYSCLK = 1 GHz (SYSCLK PLL Enabled and Driven by R&S SMA100 at 50 MHz), f_{REF} = 19.44 MHz, f_{OUT} = 155.52 MHz, SYSCLK Doubler Enabled, DPLL Loop BW = 1 kHz

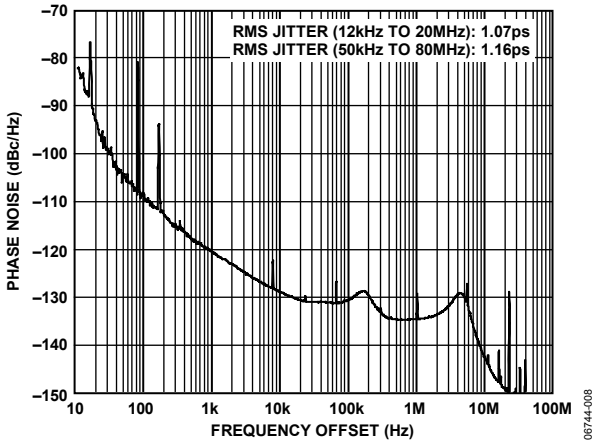


Figure 8. Additive Phase Noise at HSTL Output Driver, SYSCLK = 1 GHz (SYSCLK PLL Enabled and Driven by R&S SMA100 Signal Generator at 50 MHz), f_{REF} = 8 kHz, f_{OUT} = 155.52 MHz, DPLL Loop BW = 10 Hz

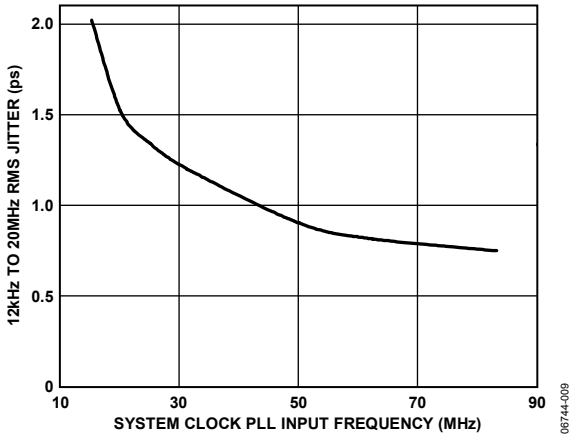


Figure 9. 12 kHz to 20 MHz RMS Jitter vs. System Clock PLL Input Frequency, SYSCLK = 1 GHz, f_{REF} = 19.44 MHz, f_{OUT} = 155.52 MHz

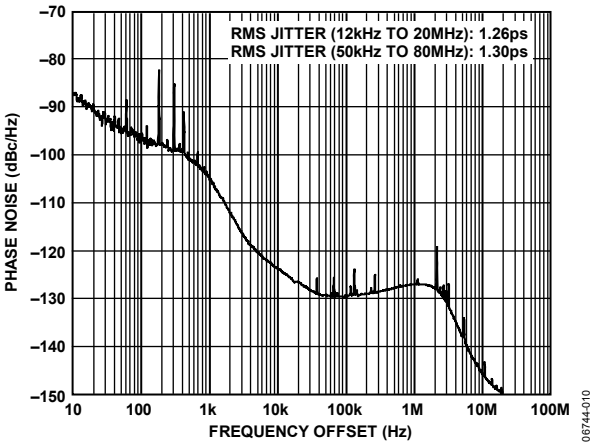


Figure 10. Additive Phase Noise at HSTL Output Driver, SYSCLK = 1 GHz (SYSCLK PLL Enabled and Driven by a 25 MHz Fox Crystal Oscillator), f_{REF} = 19.44 MHz, f_{OUT} = 155.52 MHz, DPLL Loop BW = 1 kHz

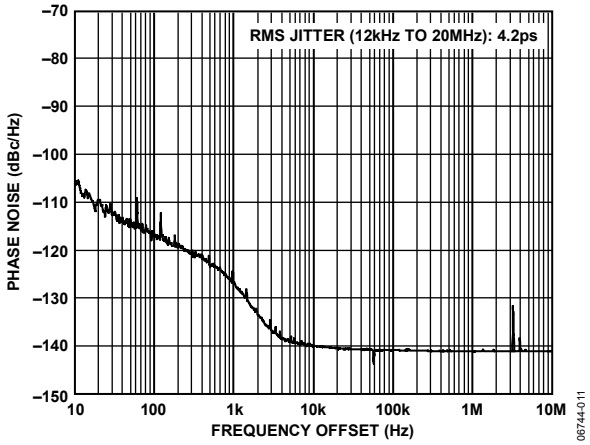


Figure 11. Additive Phase Noise at HSTL Output Driver, SYSCLK = 500 MHz (SYSCLK PLL Disabled), f_{REF} = 10.24 MHz, f_{OUT} = 20.48 MHz, DPLL Loop BW = 1 kHz

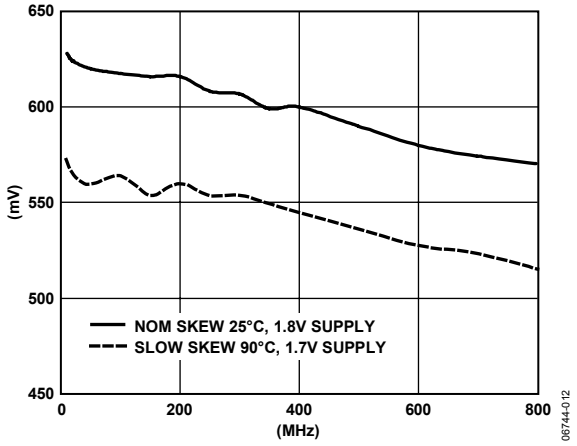


Figure 12. HSTL Output Driver Single-Ended Peak-to-Peak Amplitude vs. Toggle Rate (100 Ω Across Differential Pair)

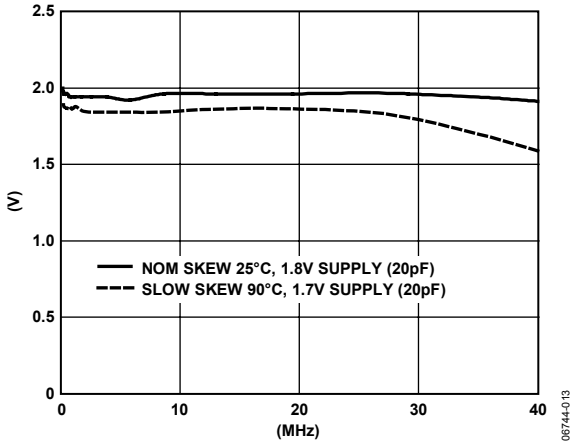


Figure 13. CMOS Output Driver Peak-to-Peak Amplitude vs. Toggle Rate (AVDD3 = 1.8 V) with 20 pF Load

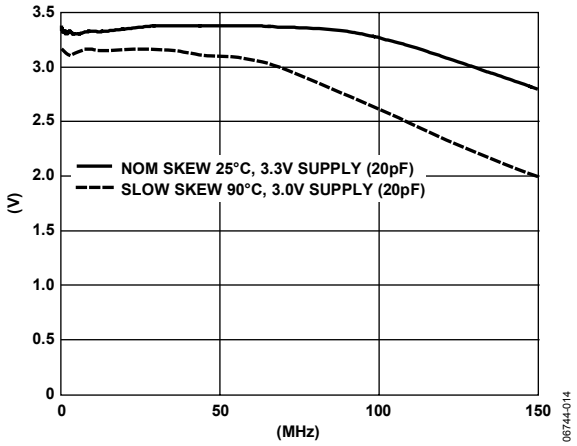


Figure 14. CMOS Output Driver Peak-to-Peak Amplitude vs. Toggle Rate (AVDD3 = 3.3 V) with 20 pF Load

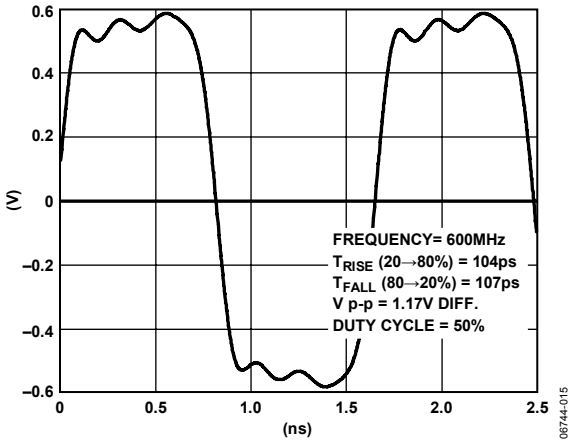


Figure 15. Typical HSTL Output Waveform, Nominal Conditions, DC-Coupled, Differential Probe Across 100 Ω load

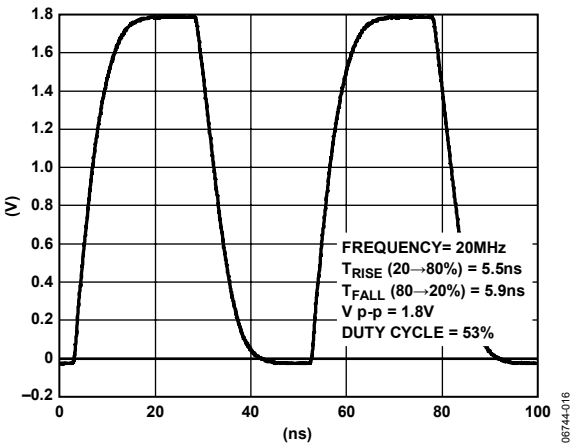


Figure 16. Typical CMOS Output Driver Waveform (@ 1.8 V), Nominal Conditions, Estimated Capacitance: 5 pF

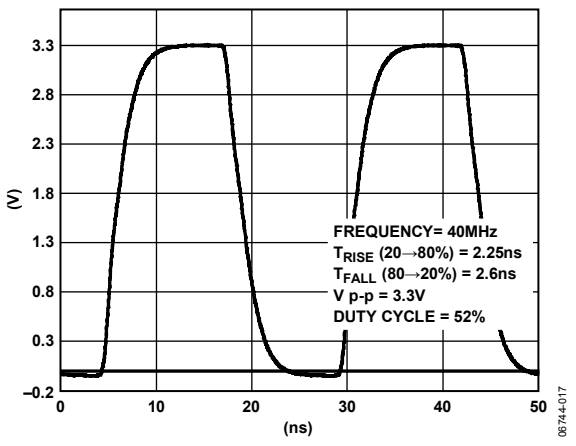


Figure 17. CMOS Output Driver Waveform (@ 3.3 V), Nominal Conditions, Estimated Capacitance: 5 pF, f_{OUT} = 20 MHz

INPUT/OUTPUT TERMINATION RECOMMENDATIONS

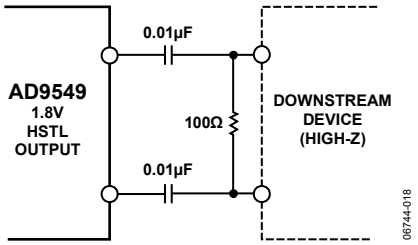


Figure 18. AC-Coupled HSTL Output Driver

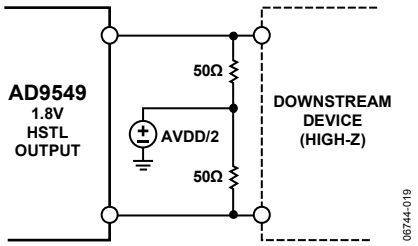


Figure 19. DC-Coupled HSTL Output Driver

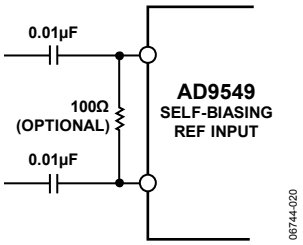


Figure 20. Reference Input

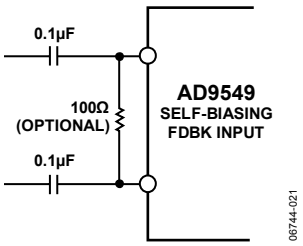


Figure 21. FDBK Input

THEORY OF OPERATION

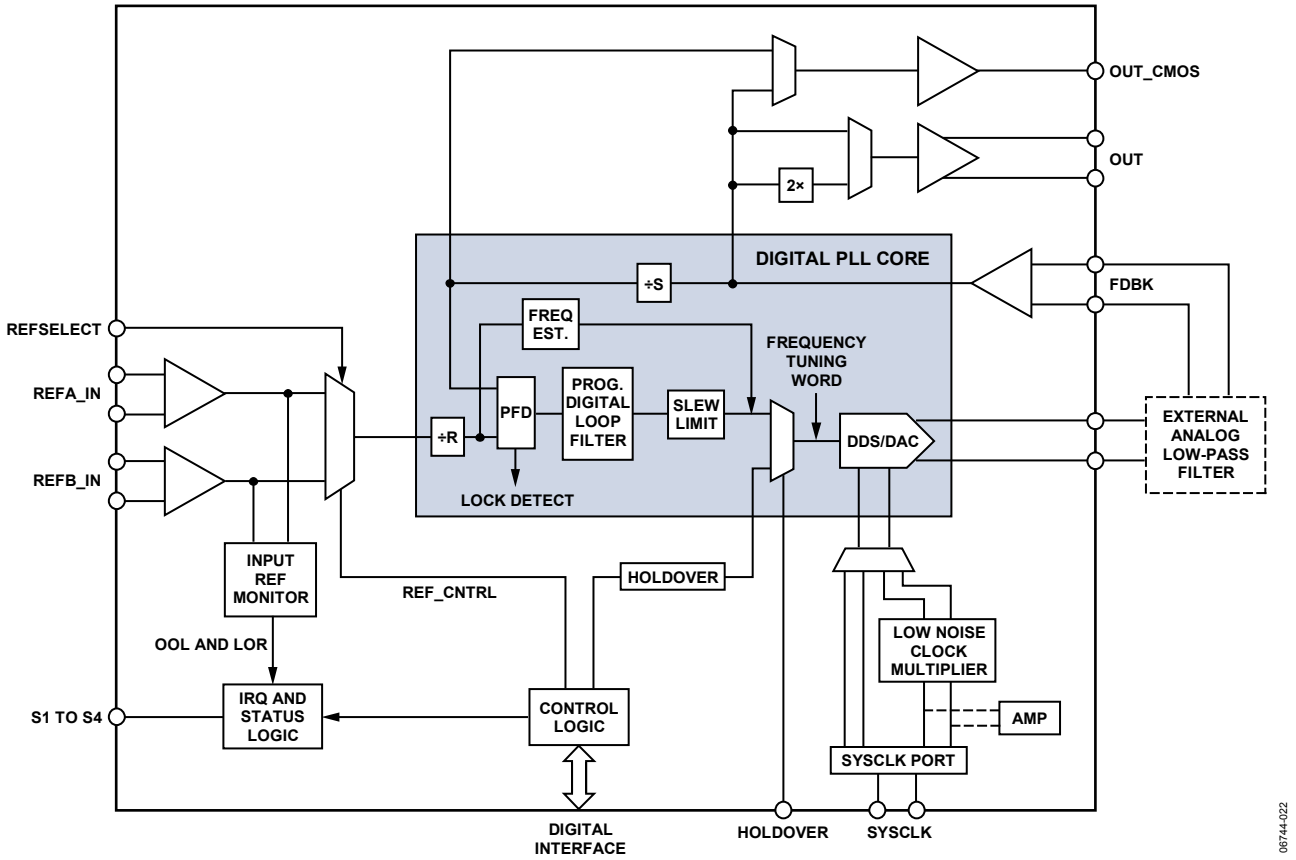


Figure 22. Detailed Block Diagram

OVERVIEW

The AD9549 provides a clocking output that is directly related in phase and frequency to the selected (active) reference (REFA or REFB) but has a phase noise spectrum primarily governed by the system clock. A wide band of reference frequencies is supported. Jitter existing on the active reference is greatly reduced by a programmable digital filter in the digital phase-locked loop (PLL), which is the core of this product. The AD9549 supports both manual and automatic holdover. While in holdover, the AD9549 continues to provide an output as long as the system clock is maintained. The frequency of the output during holdover is an average of the steady state output frequency prior to holdover.

Also offered are manual and automatic switchover modes for changing between the two references, should one become suspect or lost. A digitally controlled oscillator (DCO) is implemented using a direct digital synthesizer (DDS) with an integrated output DAC, clocked by the system clock. A bypassable PLL-based frequency multiplier is present enabling use of an inexpensive, low frequency source for the system clock. For best jitter performance, the system clock PLL should be bypassed, and a low noise, high frequency system clock should be provided directly. Sampling theory sets an upper bound for the DDS output frequency at 50% of f_S (where f_S is the DAC sample rate), but a practical limitation of 40% of f_S is generally recommended to allow for the selectivity of the required off-chip reconstruction filter. The output signal from the reconstruction filter is fed back to the AD9549, both to complete the PLL and to be processed through the output circuitry. The output circuitry includes HSTL and CMOS output buffers, as well as a frequency doubler for designs that need to provide frequencies above the Nyquist level of the DDS.

The individual functional blocks are described in the following sections.

PLL CORE (DPLLC)

The digital phase-locked loop core (DPLLC) includes the frequency estimation block and the digital phase lock control block driving the DDS.

The start of the DPLLC signal chain is the reference signal, f_R, which appears on REFA or REFB inputs. The frequency of this signal can be divided by an integer factor of R via the feedforward divider. The output of the feedforward divider is routed to the phase/frequency detector (PFD). Therefore, the frequency at the input to the PFD is given by

$$f_{PFD} = \frac{f_R}{R}$$

The PFD outputs a time series of digital words that are routed to the digital loop filter. The digital filter implementation offers many advantages: The filter response is determined by numeric coefficients rather than discrete component values. There is no aging of components and therefore, no drift of component value over time. There is no thermal noise in the loop filter, and there is no control node leakage current (which causes reference feedthrough in a traditional analog PLL).

The output of the loop filter is a time series of digital words. These words are applied to the frequency tuning input of a DDS to steer the DCO frequency. The DDS provides an analog output signal via an integrated DAC, effectively mimicking the operation of an analog VCO.

The DPLLC can be programmed to operate in conjunction with an internal frequency estimator to help decrease the time required to achieve lock. When the frequency estimator is employed, frequency acquisition is accomplished in a two-step process:

1. An estimate is made of the frequency of f_{PFD}. The phase lock control loop is essentially inoperative during the frequency estimation process. Once a frequency estimate is made, it is delivered to the DDS so that its output frequency is approximately equal to f_{PFD} multiplied by S (the modulus of the feedback divider).
2. The phase lock control loop becomes active and acts as a servo to acquire and hold phase lock with the reference signal.

As mentioned in Step 1, the DPLLC includes a feedback divider that allows the DCO to operate at an integer multiple (S) of f_{PFD}. This establishes a nominal DCO frequency (f_{DDS}), given by

$$f_{DDS} = \left(\frac{S}{R}\right) f_R$$

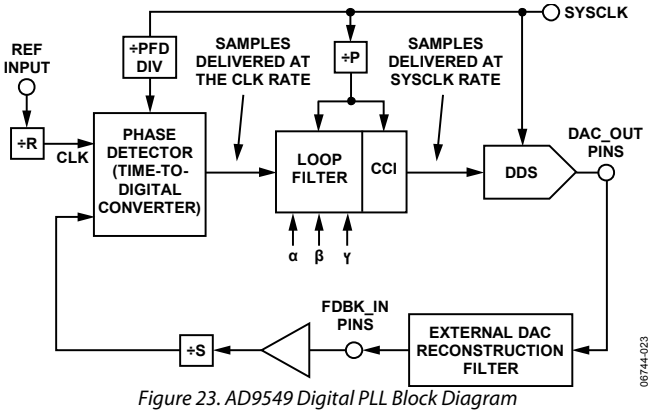


Figure 23. AD9549 Digital PLL Block Diagram

Feedforward Divider (Divide-by-R)

The feedforward divider is an integer divider that allows frequency prescaling of the REF source input signal while maintaining the desired low jitter performance of the AD9549.

The feedforward divider is a programmable modulus divider with very low jitter injection. The divider is capable of handling input frequencies as high as 750 MHz. The divider depth is 16-bits cascaded with an additional divide-by-2. The divider therefore is capable of integer division from 1 to 65,535 (index of 1) or 2 to 131,070 (index of 2). The divider is programmed via the I/O Register Map to trigger on either the rising (default) or falling edge of the REF source input signal. Note that the value stored in the R-divider register is one less than the actual R-divider, so setting the R-divider register to zero results in an R divider equal to one.

There is a lower bound on the value of R imposed by the phase frequency detector within the DPLLC, which has a maximum operating frequency of $f_{PFD[MAX]}$, as explained in the Fine Phase Detector section. The R-Divider/2 bit must be set when REFA or REFB is greater than 400 MHz. The user must also ensure that R is chosen so that it satisfies the inequality

$$R \geq \text{ceil}\left(\frac{f_R}{f_{PFD[MAX]}}\right)$$

The upper bound is

$$R \leq \text{floor}\left(\frac{f_R}{8\text{ kHz}}\right)$$

where the ceil(x) function yields the nearest integer ≥ x.

For example, if f_R=155 MHz and $f_{PFD[MAX]}$ = 24.5 MHz, then ceil (155/24.5) = 7, so R must be ≥ 7.

Feedback Divider (Divide-by-S)

The feedback divider is an integer divider allowing frequency multiplication of the REF signal that appears at the input of the phase detector. It is capable of handling frequencies well above the Nyquist limit of the DDS. The divider depth is 16-bits cascaded with an additional divide-by-2. The divider is therefore capable of integer division from 1 to 65,535 (index of 1) or 2 to 131,070 (index of 2). The divider is programmed via the I/O Register Map to trigger on either the rising (default) or falling edge of the feedback signal. Note that the value stored in the S-Divider register is one less than the actual R-divider, so setting the S-Divider register to zero results in an S-divider equal to one.

The feedback divider must be programmed within certain boundaries. The S-Divider/2 bit must be set when FDBK_IN is greater than 400 MHz. The upper boundary on the feedback divider is the lesser of the maximum programmable value of S and the maximum practical output frequency of the DDS (~ 40% f_S). Two equations are given—S_{max1} for a feedback divider index of 1 and S_{max2} for an index of 2.

$$S_{MAX1} = \min\left(\frac{40\% f_S R}{f_R}, 65{,}535\right)$$

or

$$S_{MAX2} = \min\left(\frac{40\% f_S R}{f_R}, 131{,}070\right)$$

where R is the modulus of the feedforward divider, f_S is the DAC sample rate, and f_R is the input reference frequency.

The DCO has a minimum frequency, $f_{DCO[MIN]}$ (see the DAC Output Characteristics section of the AC Specifications table). This imposes a lower bound, S_{MIN}, on the feedback divider value as well.

$$S_{MIN} = \max\left(R\left(\frac{f_{DCO[MIN]}}{f_R}\right),1\right)$$

Note that reduced DCO frequencies result in worse jitter performance (a consequence of the reduced slew rate of the sinusoid generated by the DDS).

Forward and Reverse FEC Clock Scaling

The feedforward divider (divide-by-R) and feedback divider (divide-by-S) enable FEC clock scaling. For instance, to multiply the incoming signal by 255/237, set the S-divider to 255 and the R-divider to 237. One should be careful to abide by the limitations on the R- and S-dividers, and make sure the phase detector input frequency is within specified limits.

Phase Detector

The phase detector is composed of two detectors: a coarse phase detector and a fine phase detector. The two detectors operate in parallel. Both detectors measure the duration (Δt) of the pulses generated by a conventional three-state phase/frequency detector.

Together, the fine and coarse phase detectors produce a digital word that is a time-to-digital conversion of the separation between the edge transitions of the prescaled reference signal and the feedback signal.

If the fine phase detector is able to produce a valid result, this result alone serves as the phase error measurement. If the fine phase detector is either in an overflow or underflow condition, the phase error measurement uses the coarse phase detector instead.

Digital Loop Filter

The digital loop filter integrates and low-pass filters the digital phase error values delivered by the phase detector. The loop filter response mimics that of a 2nd order RC network used to filter the output of a typical phase detector and charge pump combination as shown in Figure 24.

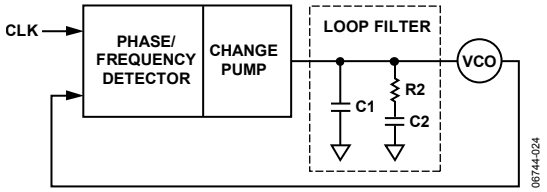


Figure 24. Typical Analog PLL Block Diagram

The building blocks implemented on the AD9549, however, are digital. A time-to-digital converter that produces digital values proportional to the edge timing error between the CLK and feedback signals replaces the phase-frequency detector and charge pump. A digital filter that processes the edge timing error samples from the time-to-digital converter replaces the loop filter. A DDS replaces the VCO, which produces a frequency that is linearly related to the digital value provided by the loop filter. This is shown in Figure 25 with some additional detail.

The samples provided by the time-to-digital converter are delivered to the loop filter at a sample rate equal to the CLK frequency (that is, f_R/R). The loop filter is intended to oversample the time-to-digital converter output at a rate determined by the P-divider. The value of P is programmable via the I/O Register Map. It is stored as a 5-bit number, P_{IO}. The value of P_{IO} is related to P by the equation

$$P = 2^{PIO}$$

where $5 \le P_{IO} \le 16$.

Hence, the P-divider can provide divide ratios between 32 and 65,536 in power-of-2 steps. With a DAC sample rate of 1 GHz, the loop filter sample rate can range from as low as 15.26 kHz to a maximum of 31.25 MHz. Coupled to the loop filter is a cascaded comb integrator (CCI) filter that provides a sample rate translation between the loop filter sample rate (f_S/P) and the DDS sample rate, f_S.

The choice of P is important because it controls both the response of the CCI filter and the sample rate of the loop filter. In order to understand the method for determining a useful value for P, it is first necessary to examine the transfer function of the CCI filter.

$$H(\omega)_{CCI} = \left[\frac{1 - e^{j\omega P}}{P(1 - e^{-j\omega}}\right]^2$$

or

$$\left|H_{CCI}(\omega)\right| = \begin{cases} 1, & \omega = 0 \\ \dfrac{1}{p_2}\left(\dfrac{1-\cos(\omega P)}{1-\cos(\omega)}\right), & \omega > 0 \end{cases}$$

To evaluate the response in terms of absolute frequency, make the substitution

$$\omega = \frac{2\pi f}{f_S}$$

where f_S is the DAC sample rate and f is the frequency at which H_{CCI} is to be evaluated.

Analysis of this function reveals that the CCI magnitude response follows a low-pass characteristic that consists of a series of P lobes. The lobes are bounded by null points occurring at frequency multiples of f_S/P. The peak of each successive lobe is lower that its predecessor over the frequency range between dc and $\frac{1}{2}f_S$. For frequencies greater than $\frac{1}{2}f_S$, the response is a reflection about the vertical at $\frac{1}{2}f_S$. Furthermore, the first lobe (which appears between dc and f_S/P) exhibits a monotonically decreasing response. That is, the magnitude is unity at dc, and it steadily decreases with frequency until it vanishes at the first null point (f_S/P).

The null points imply the existence of transmission zeros placed at finite frequencies. While transmission zeros placed at infinity yield minimal phase delay, zeros placed closer to dc result in

increased phase delay. Hence, the position of the first null point has a significant impact on the phase delay introduced by the CCI filter. This is an important consideration because excessive phase delay negatively impacts the overall closed-loop response. As a rule of thumb, choose a value for P so that the frequency of the first null point (f_S/P) is the greater of 80 times the desired loop bandwidth or 1.5 times the frequency of CLK (f_R/R).

The value of P thus calculated (P_{MAX}) is the largest usable value in practice. Because P is programmed as P_{IO}, it is necessary to define P_{MAX} in terms of P_{IO} so that P_{IOMAX} can be determined. The condition $P_{IO} \le P_{IOMAX}$ ensures that the impact of the phase delay of the CCI filter on the phase margin of the loop does not exceed 5°. P_{IOMAX} can be expressed as

$$P_{IOMAX} = \max\left\langle 5, \min\left\{ 16, \text{floor}\left[\log_2\left(\frac{f_S}{80 f_{LOOP}} \right) \right], \text{floor}\left[\log_2\left(\frac{2 f_S}{3 f_{REF}} \right) \right] \right\} \right\rangle$$

With a properly chosen value for P, the closed-loop response of the digital PLL is primarily determined by the response of the digital loop filter. Flexibility in controlling the loop filter response translates directly into flexibility in the range of applications satisfied by the architecture of the AD9549.

The AD9549 evaluation software automatically sets the value of the P-divider based on the user's input criteria. Therefore, the formulas are provided here mainly to assist in understanding how the part works.

Direct Digital Synthesizer

One of the primary building blocks of the digital PLL is a direct digital synthesizer (DDS). The DDS behaves like a sinusoidal signal generator. The frequency of the sinusoid generated by the DDS is determined by a frequency tuning word (FTW), which is a digital (that is, numeric) value. Unlike an analog sinusoidal generator, a DDS uses digital building blocks and operates as a sampled system. Thus, it requires a sampling clock (f_S) that serves as the DDS's fundamental timing source. The accumulator behaves as a modulo-2^{48} counter with a programmable step size (FTW). A block diagram of the DDS is shown in Figure 25.

The input to the DDS is a 48-bit FTW that provides the accumulator with a seed value. On each cycle of f_S, the accumulator adds the value of the FTW to the running total of its output. For example, given an FTW = 5, the accumulator counts by 5s, incrementing on each f_S cycle. Over time, the accumulator reaches the upper end of its capacity (2^{48} in this case), at which point, it rolls over, retaining the excess. The average rate at which the accumulator rolls over establishes the frequency of the output sinusoid. The average rollover rate of the accumulator is given by the next equation and establishes the output frequency (f_{DDS}) of the DDS.

$$f_{DDS} = \left(\frac{FTW}{2^{48}} \right) f_S$$

Solving this equation for FTW yields

$$FTW = \text{round}\left[2^{48} \left(\frac{f_{DDS}}{f_S} \right) \right]$$

For example, given that f_S = 1 GHz and f_{DDS} = 19.44 MHz, then FTW = 5,471,873,547,255 (0x04FA05143BF7).

The relative phase of the sinusoid can be controlled numerically, as well. This is accomplished using the phase offset input to the DDS (a programmable 16-bit value (Δphase); see the I/O Register Map section). The resulting phase offset, ΔΦ (radians), is given by

$$\Delta\Phi = 2\pi\left(\frac{\Delta phase}{2^{16}} \right)$$

The DDS can be operated in either open-loop or closed-loop mode, via the Close Loop bit in the DPLL Register.

There are two open-loop modes: single tone and holdover. In single tone mode, the DDS behaves like a frequency synthesizer, and uses the value stored in the FTW0 register to determine its output frequency. Alternatively, the FTW and Δphase values can be determined by the device itself using the frequency estimator. Because single tone mode ignores the reference inputs, it is very useful for generating test signals to aid in debugging. Single tone mode must be activated manually via register programming.

In holdover mode, the AD9549 uses past tuning words when the loop is closed to determine its output frequency. Therefore, the loop must have been successfully closed in order for holdover mode to work. Switching in and out of holdover mode can be either automatic or manual, depending on register settings.

Typically, the AD9549 operates in closed-loop mode. In closed-loop mode, the FTW values come from the output of the digital loop filter and vary with time. The DDS frequency is steered in a manner similar to a conventional VCO-based PLL.

Note that in closed-loop mode, the DDS phase offset capability is inoperative.

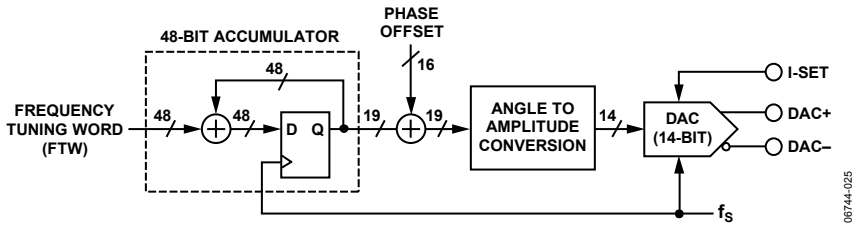


Figure 25. DDS Block Diagram

DAC Output

The output of the digital core of the DDS is a time series of numbers representing a sinusoidal waveform. This series is translated to an analog signal by means of a digital-to-analog converter (DAC).

The DAC outputs its signal to two pins driven by a balanced current source architecture (see theDAC output diagram in Figure 26). The peak output current derives from the combination of two factors. The first is a reference current (I_{DAC_REF}) established at the DAC_RSET pin and the second is a scale factor programmed into the I/O register map.

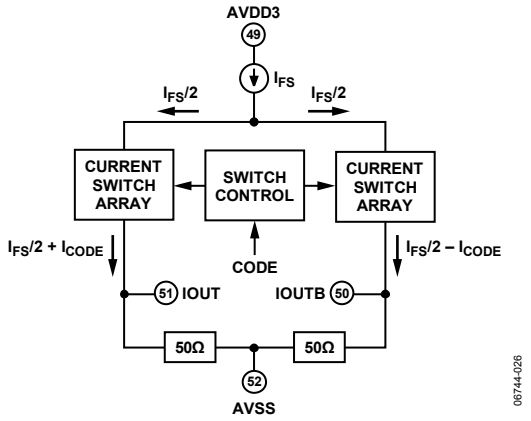


Figure 26. DAC Output Pins

The value of I_{DAC_REF} is set by connecting a resistor (R_{DAC_REF}) between the DAC_RSET pin and ground. The DAC_RSET pin is internally connected to a virtual voltage reference of 1.2 V nominal, so the reference current can be calculated by

$$I_{DAC\_REF} = \frac{1.2}{R_{DAC\_REF}}$$

Note that the recommended value of I_{DAC_REF} is 120 μA, which leads to a recommended value for R_{DAC_REF} of 10 kΩ.

The scale factor consists of a 10-bit binary number (FSC) programmed into the DAC Full-Scale Current register in the I/O register map. The full-scale DAC output current (I_{DAC_FS}) is given by

$$I_{DAC\_FS} = I_{DAC\_REF}\left(72 + \frac{192FSC}{1024}\right)$$

Using the recommended value of R_{DAC_REF}, the full-scale DAC output current can be set with 10-bit granularity over a range of approximately 8.6 mA to 31.7 mA. 20 mA is the default value.

PHASE DETECTOR

Coarse Phase Detector

The coarse phase detector uses the DAC sample rate (f_S) to determine the edge timing deviation between the REF signal and the feedback signal generated by the DDS. Hence, f_S sets the timing resolution of the coarse phase detector. At the recommended rate of f_S = 1 GHz, the coarse phase detector spans a range of over 131 μs (sufficient to accommodate REF signal frequencies as low as 8 kHz).

The phase gain of the coarse phase detector is controlled via the I/O registers by means of two numeric entries. The first is a 3-bit power-of-2 scale factor, PDS. The second is a 6-bit linear scale factor, PDG.

$$PhaseGain_{CPD} = R\left(\frac{f_S}{f_R}\right)\left(2^{PDS+6}\,PDG\right)$$

Fine Phase Detector

The fine phase detector operates on a divided down version of f_S as its sampling time base. The sample rate of the fine phase detector is set using a 4-bit word (PFD_Div) in the I/O register map and is given by

$$Fine\ Phase\ Detector\ Sample\ Rate = \frac{f_S}{4(PFD\_Div)}$$

The default value of PFD_Div is 5, so for f_S = 1 GHz, the default sample rate of the fine phase detector is 50 MHz. The upper bound on the maximum allowable input frequency to the phase detector ($f_{PFD[MAX]}$) is 49% of the sample rate, or

$$f_{PFD[MAX]} = \frac{f_S}{8(PFD\_Div)}$$

Therefore, $f_{PFD[MAX]}$ is 25 MHz in the preceding example.

The fine phase detector uses a proprietary technique to determine the phase deviation between the REF signal and feedback signal.

The phase gain of the fine phase detector is controlled by an 8-bit scale factor (FPFD_Gain) in the I/O register map. The nominal (default) value of FPFD_Gain is 200, and establishes the phase gain as

$$PhaseGain_{FP}D = \frac{R(2^{10} \times 10^7)(FPFD\_Gain)}{f_R}$$

Phase Detector Gain Matching

Although the fine and coarse phase detectors use different means to make a timing measurement, it is essential that both have equivalent phase gain. Without proper gain matching, the closed-loop dynamics of the system cannot be properly controlled. Hence, the goal is to make $PhaseGain_{CPD} = PhaseGain_{FPD}$. This leads to

$$(f_S 2^{PDS+6})PDG = (2^{10} \times 10^7)FPFD\_Gain$$

which simplifies to

$$2^{PDS}\,PDG = \frac{(16 \times 10^7)FPFD\_Gain}{f_S}$$

Typically, FPFD_Gain is established first and then PDG and PDS are calculated. The proper choice for PDS is given by

$$PDS = \text{round}\left[\log_2\left(\frac{10^7 \times FPFD\_Gain}{2f_S}\right)\right]$$

The final value of PDS must satisfy 0 ≤ PDS ≤ 7. The proper choice for PDG is calculated using the following equation:

$$PDG = \text{round}\left(\frac{10^7\, FPFD\_Gain}{2^{PDS-4} f_S}\right)$$

The final value of PDG must satisfy 0 ≤ PDG ≤ 63. For example, let f_S = 700 MHz and FPFD_Gain = 200, then PDS = 1 and PDG = 23.

Note that the AD9549 evaluation software calculates register values that have the phase detector gains already matched.

Phase Detector Pin Connections

There are three pins associated with the phase detector that must be connected to external components. Figure 27 shows the recommended component values and their connections.

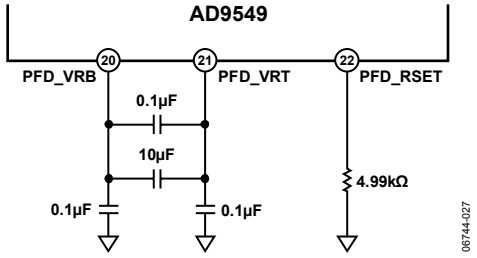


Figure 27. Phase Detector Pin Connections

DIGITAL LOOP FILTER COEFFICIENTS

In order to provide the desired flexibility, the loop filter has been designed with three programmable coefficients (α, β, and γ). The coefficients along with P (where P = 2^{PIO}) completely define the response of the filter, which is given by

$$H(\omega)_{LoopFilter} = \alpha\left(\frac{e^{j\omega} + (\beta - \gamma - 1)}{e^{j2\omega} + (-\gamma - 2)e^{j\omega} + (\gamma + 1)}\right)$$

To evaluate the response in terms of absolute frequency, substitute

$$\omega = \frac{2\pi Pf}{f_S}$$

where *P* is the divide ratio of the P-divider, f_S is the DAC sample rate, and *f* is the frequency at which the function is to be evaluated.

The loop filter coefficients are determined by the AD9549 evaluation software according to three parameters:

- Φ is the desired closed-loop phase margin (0 < Φ < π/2 rad).
- f_{LOOP} is the desired open-loop bandwidth (Hz).
- f_{DDS} is the desired output frequency of the DDS (Hz). Note that f_{DDS} can also be expressed as $f_{DDS} = f_R(S/R)$.

The three coefficients are calculated according to parameters via the following equations:

$$\beta = -4\pi Pf_C \tan(\Phi)$$

$$\gamma = \tfrac{1}{2} F(\Phi)\beta$$

$$\alpha = -\left(\frac{2^{38}\pi}{10^7\, FPFD\_Gain}\right) f_{DDS} f_C F(\Phi)\beta$$

where:

$$F(\Phi) = 1 + \frac{1}{\sin(\Phi)}$$

$$f_C = \frac{f_{LOOP}}{f_S}$$

FPFD_Gain is the value of the gain scale factor for the fine phase detector as programmed into the I/O register map.

Note that the range of loop filter coefficients is limited as follows:

$0 < \alpha < 2^{23}$ (~8.39×10^6)
$-0.125 < \beta < 0$
$-0.125 < \gamma < 0$

The preceding constraints on β and γ constrain the closed-loop phase margin such that both β and γ assume negative values. Even though β and γ are limited to negative quantities, the values as programmed are positive. The negative sign is assumed internally.

Note that the closed-loop phase margin is limited to the range of 0° < Φ < 90° because β and γ are negative.

The three coefficients are implemented as digital elements, necessitating quantized values. Determination of the programmed coefficient values in this context follows.

The quantized α coefficient is composed of three factors, where α_0, α_1, and α_2 are the programmed values for the α coefficient.

$$\alpha_{QUANTIZED} = \left(\frac{\alpha_0}{2048}\right)\left(2^{\alpha_1}\right)\left(2^{-\alpha_2}\right)$$

The boundary values for each are $0 \le \alpha_0 \le 4095$, $0 \le \alpha_1 \le 22$, and $0 \le \alpha_2 \le 7$. The optimal values of α_0, α_1, and α_2 are

$$\alpha_1 = \max\left[0, \min\left\{22, \text{ceil}\left(\log_2\frac{2048\alpha}{4095}\right)\right\}\right]$$

$$\alpha_2 = \max\left[0, \min\left\{7, \text{floor}\left(\log_2\left(\frac{4095}{\alpha}\right) + \alpha_1 - 11\right)\right\}\right]$$

$$\alpha_0 = \max\left[0, \min\left\{4095, \text{round}\left(\alpha \times 2^{\alpha_2 - \alpha_1 + 11}\right)\right\}\right]$$

The magnitude of the quantized β coefficient is composed of two factors.

$$\beta_{QUANTIZED} = \left(\beta_0\right)\left(2^{-(\beta_1 + 15)}\right)$$

where β_0 and β_1 are the programmed values for the β coefficient.

The boundary values for each are $0 \le \beta_0 \le 4095$ and $0 \le \beta_1 \le 7$. The optimal values of β_0 and β_1 are

$$\beta_1 = \max\left[0, \min\left\{7, \text{floor}\left(\log_2\left(\frac{4095}{|\beta|}\right) - 15\right)\right\}\right]$$

$$\beta_0 = \max\left[0, \min\left\{4095, \text{round}\left(|\beta| \times 2^{\beta_1 + 15}\right)\right\}\right]$$

The magnitude of the quantized γ coefficient is composed of two factors.

$$\gamma_{QUANTIZED} = (\gamma_0)\left(2^{-(\gamma_1 + 15)}\right)$$

where γ_0 and γ_1 are the programmed values for the γ coefficient; the boundary values for each are $0 \le \gamma_0 \le 4095$ and $0 \le \gamma_1 \le 7$. The optimal values of γ_0 and γ_1 are

$$\gamma_1 = \max\left[0, \min\left\{7, \text{floor}\left(\log_2\left(\frac{4095}{|\gamma|}\right) - 15\right)\right\}\right]$$

$$\gamma_0 = \max\left[0, \min\left\{4095, \text{round}\left(|\gamma| \cdot 2^{\gamma_1 + 15}\right)\right\}\right]$$

The min(), max(), floor(), ceil() and round() functions are defined as follows:

- The function $\min(x_1, x_2, \ldots x_n)$ chooses the smallest value in the list of arguments.
- The function $\max(x_1, x_2, \ldots x_n)$ chooses the largest value in the list of arguments.
- The function ceil(x) increases x to the next higher integer if x is not an integer; otherwise, x is unchanged.
- The function floor(x) reduces x to the next lower integer if x is not an integer; otherwise, x is unchanged.
- The function round(x) rounds x to the nearest integer.

To demonstrate the wide programmable range of the loop filter bandwidth, consider the following design example. The system clock frequency (f_S) is 1 GHz, the input reference frequency (f_R) is 19.44 MHz, the DDS output frequency (f_{DDS}) is 155.52 MHz, and the required phase margin (Φ) is 45°. f_R is within the nominal bandwidth of the phase detector (25 MHz), and f_{DDS}/f_R is an integer (8), so the prescaler is not required. Therefore, R = 1 and S = 8 can be used for the feedforward and feedback dividers, respectively.

Note that if f_{DDS}/f_R is a noninteger, then R and S must be chosen such that $S/R = f_{DDS}/f_R$ with S and R both constrained to integer values. For example, if f_R = 10 MHz and f_{DDS} = 155.52 MHz, then the optimal choice for S and R is 1944 and 125, respectively.

The open-loop bandwidth range under the defined conditions spans 9.5 Hz to 257.5 kHz. The wide dynamic range of the loop filter coefficients allows for programming of any open-loop bandwidth within this range under these conditions. The resulting closed-loop bandwidth range under the same conditions is approximately 12 Hz to 359 kHz.

The resulting loop filter coefficients for the upper loop bandwidth along with the necessary programming values are shown as follows:

α = 4322509.4784981
α_0 = 2111 (0x83F)
α_1 = 22 (0x16)
α_2 = 0 (0x00)
β = −0.10354689386232
β_0 = 3393 (0xD41)
β_1 = 0 (0x00)
γ_0 = 4095 (0xFFF)
γ = −0.12499215775201
γ_1 = 0 (0x00)

The resulting loop filter coefficients for the lower loop bandwidth along with the necessary programming values are shown as follows:

α = 0.005883404361345
α_0 = 1542 (0x606)
α_1 = 0 (0x00)
α_2 = 7 (0x07)
β = −0.000003820176667
β_0 = 16 (0x10)
β_1 = 7 (0x07)
γ = −0.00000461136116
γ_0 = 19 (0x13)
γ_1 = 7 (0x07)

The AD9549 evaluation software generates these coefficients automatically based on the user's desired loop characteristics.

CLOSED-LOOP PHASE OFFSET

The AD9549 provides for limited control over the phase offset between the reference input signal and the output signal by adding a constant phase offset value to the output of the phase detector. An adder is included at the output of the phase detector as shown in Figure 28 to support this. The value of the constant (PLL_{OFFSET}) is set via the PLL Offset register.

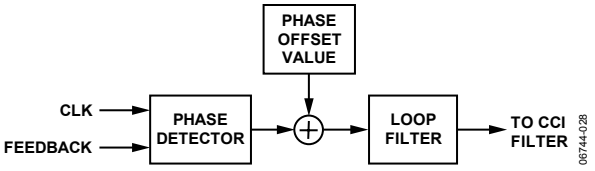


Figure 28. Input Phase Offset Adder

PLL_{OFFSET} is a function of the phase detector gain and the desired amount of timing offset (Δt_{OFFSET}). It is given by

$$P_{LLOFFSET} = \Delta t_{OFFSET}\left(2^{10} \times 10^7 \times FPFD\_Gain\right)$$

FPFD_Gain is described in the Fine Phase Detector section.

For example, suppose that FPFD_Gain = 200, f_{CLK} = 3 MHz, and 1° of phase offset is desired. First, the value of Δt_{OFFSET} must be determined, which is

$$\Delta t_{OFFSET} = \frac{\text{deg}}{360} t_{CLK} = \frac{1}{360}\left(\frac{1}{3\text{ MHz}}\right) = 925.9\text{ ps}$$

Having determined Δt_{OFFSET},

$$PLL_{OFFSET} = 925.9 \text{ ps}(2^{10} \times 10^7 \times 200) = 1896$$

The result has been rounded because PLL_{OFFSET} is restricted to integer values.

Note that the PLL_{OFFSET} value is programmed as a 14-bit, twos complement number. However, the user must ensure that the magnitude is constrained to 12 bits, such that:

$$-2^{11} \leq PLL_{OFFSET} < +2^{11}$$

The preceding constraint yields a timing adjustment range of ±1 ns. This ensures that the phase offset remains within the bounds of the fine phase detector.

LOCK DETECTION

Phase Lock Detection

During the phase locking process, the output of the phase detector tends toward a value of zero, which indicates perfect alignment of the phase detector input signals. As the control loop works to maintain the alignment of the phase detector input signals, the output of the phase detector wanders around zero.

The phase lock detector tracks the absolute value of the digital samples generated by the phase detector. These samples are compared to the phase lock detect threshold value (PLDT) programmed in the I/O register map. A false state at the output of the comparator indicates that the absolute value of a sample exceeds the value in the threshold register. A true state at the output of the comparator indicates alignment of the phase detector input signals to the degree specified by the lock detection threshold.

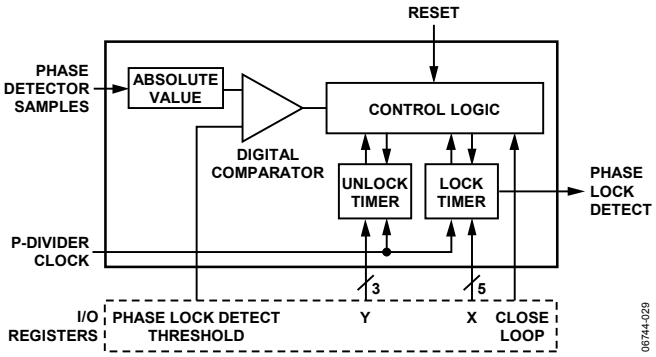


Figure 29. Phase Lock Detector Block Diagram

The phase lock detect threshold value is a 32-bit number stored in the I/O register map.

$$PLDT = \text{round}\left(\Delta t \times 2^{10} \times 10^7 \times FPFD\_Gain\right)$$

where Δt is the maximum allowable timing error between the signals at the input to the phase detector and the value of *FPFD_Gain* is as described in the Fine Phase Detector section.

For example, suppose that f_R/R = 3 MHz, FPFD_Gain = 200, and the maximum timing deviation is given as 1°. This yields a Δt value of

$$\Delta t = \frac{1^\circ}{360^\circ}\left(R \times T_R\right) = \frac{R}{360 f_R} = \frac{1}{360(3 \times 10^6)}$$

The resulting phase lock detect threshold is

$$PLDT = \text{round}\left(\frac{2^{10} \times 10^7 \times 200}{360(3 \times 10^6)}\right) = 1896$$

Hence, 1896 (0x00000768) is the value that must be stored in the Phase Lock Detect Threshold register.

The phase lock detect signal is generated once the control logic observes that the output of the comparator has been in the true state for 2^x periods of the P-divider clock (see the Digital Loop Filter section for a description of the P-divider). Once the phase lock detect signal is asserted, it remains asserted until cleared by an unlock event or by a device reset.

The duration of the lock detection process is programmable via the Phase Lock Watchdog Timer register. The interval is controlled by a 5-bit number, X (0 ≤ X ≤ 20). The absolute duration of the phase lock detect interval is

$$t_{LOCK} = \frac{2^X P}{f_S}$$

Hysteresis in the phase lock detection process is controlled by specifying the minimum duration that qualifies as an unlock event. An unlock event is declared when the control logic observes that the output of the comparator has been in the false state for 2^{Y+1} periods of the P-divider clock (provided that the phase lock detect signal has been asserted). Detection of an unlock event clears the phase lock detect signal, and the phase lock detection process is automatically restarted.

The time required to declare an unlock event is programmable via the Phase Unlock Watchdog Timer register. The interval is controlled by a 3-bit number, Y (0 ≤ Y ≤ 7). The absolute duration of the unlock detection interval is

$$t_{UNLOCK} = \frac{2^{Y+1} P}{f_S}$$

Figure 30 shows the basic timing relationship between the reference signal at the input to the phase detector, the phase error magnitude, the output of the comparator, and the output of the phase lock detector. The example shown here assumes that X = 3 and Y = 1.

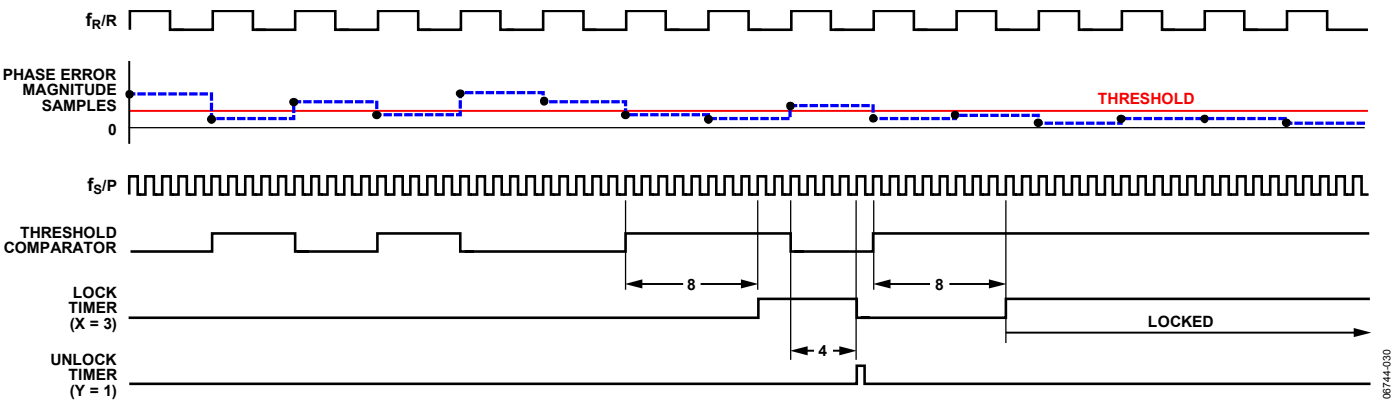


Figure 30. Lock/Unlock Detection Timing

Frequency Lock Detection

Frequency lock detection is similar to phase lock detection, with the exception that the difference between successive phase samples is the source of information. A running difference of the phase samples serves as a digital approximation to the time-derivative of the phase samples, which is analogous to frequency.

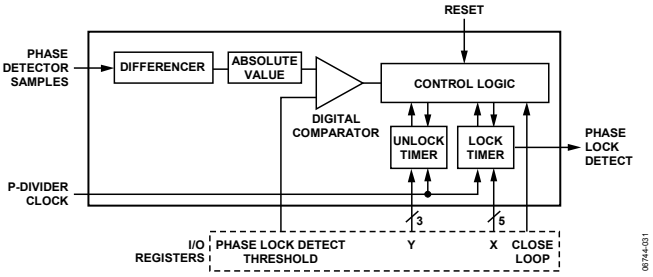


Figure 31. Frequency Lock Detection

The formula for the frequency lock detect threshold value (FLDT) is

$$FLDT = \text{round}\left[\Delta f \times 2^{10} \times 10^{7} \times FPFD\_Gain\left(\frac{R}{f_R}\right)^2\right]$$

where f_R is the frequency of the active reference, R is the value of the reference prescaler, and Δf is the maximum frequency deviation of f_R that is considered to indicate a frequency-locked condition ($\Delta f \geq 0$).

For example, suppose that f_R = 3 MHz, R = 5, FPFD_Gain = 200, and a frequency lock threshold of 1% is specified. Then, the frequency lock detect threshold value is

$$FLDT = \text{round}\left[\left(1\% \times 3 \times 10^{6}\right) \times 2^{10} \times 10^{7} \times 200 \times \left(\frac{5}{3 \times 10^{6}}\right)^2\right] = 170{,}667$$

Hence, 170,667 (0x00029AAB) is the value that should be stored in the Frequency Lock Detect Threshold register.

The duration of the frequency lock/unlock detection process is controlled in exactly the same way as the phase lock/unlock detection process in the previous section. However, different control registers are used—the Frequency Lock/Unlock Watchdog Timer registers.

REFERENCE MONITORS

Loss of Reference

The AD9549 can set an alert when one or both of the reference signals are not present. Each of the two reference inputs (REFA, REFB) has a dedicated LOR (loss of reference) circuit enabled via the I/O register map. Detection of an LOR condition sets the appropriate LOR bit in both a status register and an IRQ register in the I/O register map. The LOR state is also internally available to the multipurpose status pins (S1 to S4) of the AD9549. By setting the appropriate bit in the I/O register map, the user can assign a status pin to each of the LOR flags. This provides a means to control external hardware based on the state of the LOR flags directly.

The LOR circuits are internal watchdog timers with a programmable period. The period of the timer is set via the I/O register map so that its period is longer than that of the monitored reference signal. The rising edge of the reference signal continuously resets the watchdog timer. If the timer reaches a full count, this indicates that the reference was either lost or its period was longer than the timer period. LOR does not differentiate between these.

The period for each of the LOR timers is controlled by a 16-bit word in the I/O register map. The period of the timer clock (t_{CLK}) is $2/f_S$. Therefore, the period of the watchdog timer (t_{WD}) is

$$t_{WD} = (2/f_S)N$$

where N is the value of the 16-bit word stored in the I/O register map for the appropriate LOR circuit.

Choose the value of N so that the watchdog period is greater than the input reference period, expressed mathematically as

$$N > floor\left(\frac{f_S}{2f_R}\right)$$

where f_R is the frequency of the input reference.

The value of N results in establishing two frequencies—one for which the LOR signal is never triggered ($f_{PRESENT}$), and one for which the LOR signal is always active (f_{LOST}). Between these frequencies, the LOR signal intermittently toggles between states.

The values of the two frequency bounds are

$$f_{PRESENT} = \frac{f_S}{2N}$$

$$f_{LOST} = \frac{f_S}{2(N+1)}$$

Note that when N is chosen to be $\text{floor}\left(\frac{f_S}{2f_R}\right)+1$,

the LOR circuit is capable of indicating an LOR condition in little more than a single input reference period. For example, if f_S = 1 GHz and f_R = 2.048 MHz, then the smallest usable N value is

$$N_{MIN} = \text{floor}\left(\frac{10^9}{2(2.048\times10^6)}\right)+1 = 245$$

This yields the following values for $f_{PRESENT}$ and f_{LOST}:

$f_{PRESENT}$ = 2,048,816

f_{LOST} = 2,032,520

Note that N should be chosen sufficiently large to account for any acceptable deviation in the period of the input reference signal.

Notice that the value of N is inversely proportional to the reference frequency, meaning that as the reference frequency goes up, the precision for adjusting the threshold goes down. Proper operation of the LOR circuit requires that N be no less than 3. Therefore, the highest reference frequency for which the LOR circuit functions properly is given by

$$f_{LOR[MAX]} = \frac{f_S}{6}$$

Reference Frequency Monitor

The AD9549 can set an alert whenever one or both of the reference inputs drift in frequency beyond user-specified limits. Each of the two references has a dedicated out of limits (OOL) circuit enabled/disabled via the I/O register map. Detection of an OOL condition sets the appropriate OOL bit in both a status register and an IRQ register in the I/O register map. The user can also assign a status pin (S1 to S4) to each of the OOL flags by setting the appropriate bit in the I/O register map. This provides a means to control external hardware based on the state of the OOL flags directly.

Each reference monitor contains three main building blocks: a programmable reference divider, a 32-bit counter, and a 32-bit digital comparator.

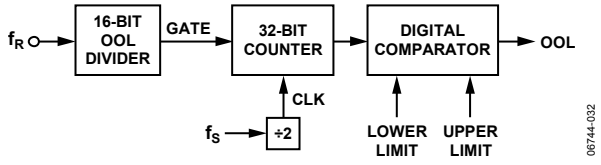


Figure 32. Reference Monitor

Four values are needed to calculate the correct values of the reference monitor: the system clock frequency, f_S (usually 1 GHz), the reference input frequency, f_R (in Hz), the error bound, E (1% = 0.01), and the monitor window size (W). The monitor window size is the difference between the maximum and minimum number of counts accumulated between adjacent edges of the reference input. If this window is too small, random variations cause the OOL detector to indicate incorrectly that a reference is out of limits. However, the time required to determine if the reference frequency is valid increases with window size. A window size of at least 20 is a good starting point.

The four input values mentioned previously are used to calculate the OOL divider (D) and OOL nominal value (N), which in turn are used to calculate the OOL upper limit (U) and OOL lower limit (L) according to the following formulas:

$$D = \max\left[1, \min\left(65{,}535, \text{ceil}\left(4\times\frac{f_R}{f_S}\times\frac{W}{E}\right)\right)\right]$$

$$N = \frac{f_R}{f_S}\times\frac{D}{4}$$

$$L = \text{floor}(N) - \text{floor}(W)$$

$$U = \text{ceil}(N) + \text{floor}(W)$$

The timing accuracy is dependent on two factors. The first is the inherent accuracy of f_S because it serves as the time base for the reference monitor. As such, the accuracy of the reference monitor can be no better than the accuracy of f_S. Second, the value of W, which must be sufficiently large so that the timer resolves the deviation between a nominal value of f_R and a value that is out of limits.

As an example, let f_R = 10 MHz, E = 1.0%, f_S = 1 GHz, and W = 20. The limits are then

Lower Limit = 1980
Upper Limit = 2020

Now let E = 0.01%. Then the limits are

Lower Limit = 199980
Upper Limit = 200020

Notice that the number of counts (and time) required to make this measurement has increased 100×.

REFERENCE SWITCHOVER

The AD9549 supports dual input reference clocks. Reference switchover can be accomplished either automatically or manually by appropriately programming the Automatic Selector bit in the I/O register map. Transition to a newly selected reference depends on a number of factors:

- State of the REFSELECT pin
- State of the REF_AB control register bit
- State of the Enable Ref Input Override register bit
- Holdover status

A functional diagram of the reference switchover and holdover logic is shown in Figure 33.

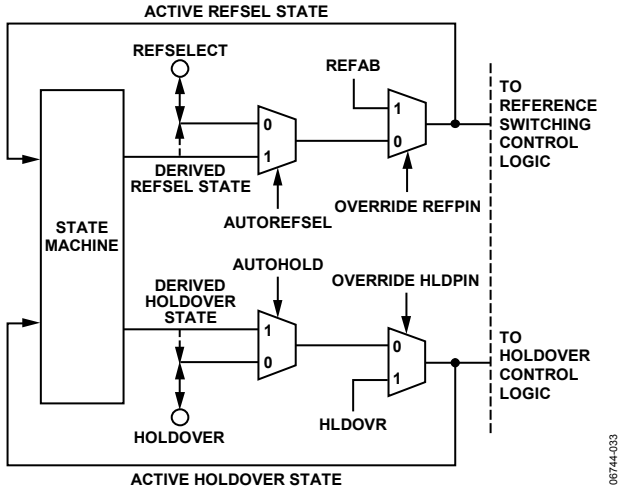


Figure 33. Reference Switchover and Holdover Logic

In manual mode, the active reference is determined by an externally applied logic level to the REFSELECT pin. In automatic mode, an internal state machine determines which reference is active, and the REFSELECT pin becomes an output indicating which reference the state machine is using.

The user can override the active reference chosen by the internal state machine via the Enable Ref Input Override bit in the I/O register map. The REF_AB bit in the I/O register map is then used to select the desired reference. When in override, it is important to note that the REFSELECT pin does not indicate the physical reference selected by the REF_AB bit. Instead, it indicates the reference that the internal state machine would select if the device were not in the override mode. This allows the user to force a reference switchover by means of the programming registers while monitoring the response of the state machine via the REFSELECT pin.

The same type of operation (manual/automatic and override) also applies to the holdover function, as shown in the reference switchover logic diagram (Figure 33). The dashed arrows in the diagram indicate that the state machine output is available to the REFSELECT and HOLDOVER pins when in override mode.

Use of Line Card Mode to Eliminate Runt Pulses

When two references are not in exact phase alignment and a transition is made from one to the other, it is possible that an extra pulse can be generated. This depends on the relative edge placement of the two references and the point in time that a switchover is initiated. To eliminate the extra pulse problem, an Enable Line Card Mode bit is provided in the I/O Register map. The line card mode logic is shown in Figure 34. When the Enable Line Card bit is 0, reference switchover occurs on command without consideration to the relative edge placement of the references. This means that there is the possibility of an extra pulse. However, when this bit is set to 1, the timing of the reference switchover is executed conditionally, as shown in Figure 35.

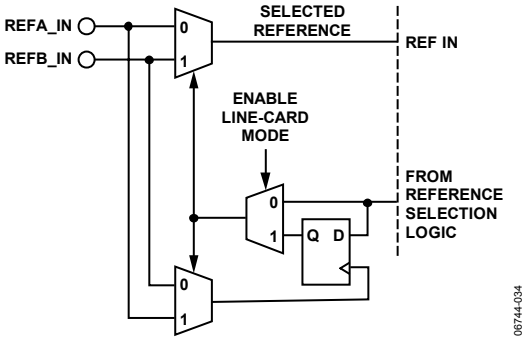


Figure 34. Reference Switchover Control Logic

Note that when the line card mode is enabled, the rising edges of the alternate reference are used to clock a latch. The latch holds off the actual transition until the next rising edge of the alternate reference.

Shown in Figure 35 is a timing diagram that demonstrates the difference between reference switchover with the line card mode enabled and disabled. If enabled, when the reference switchover logic is given the command to switch to the alternate reference, an actual transition does not occur until the next rising edge of the alternate reference. This action eliminates the spurious pulse that can occur when the line card mode is disabled.

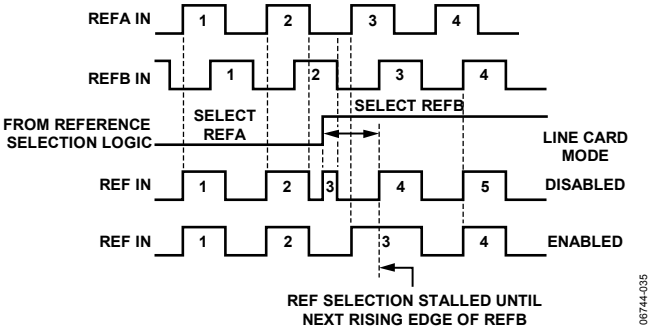


Figure 35. Reference Switchover Timing

Effect of Reference Input Switchover on Output Clock

The section covers the transient behavior of the AD9549 during a clock switchover event. This is also applicable when the AD9549 leaves holdover and reverts to being locked to a reference input. There is no phase disturbance entering holdover mode.

Switching reference inputs with different phases causes a transient frequency disturbance at the output of the PLL. The magnitude of this disturbance depends on the frequency of the reference inputs, the magnitude of the phase offset between the two references, and the digital PLL loop bandwidth.

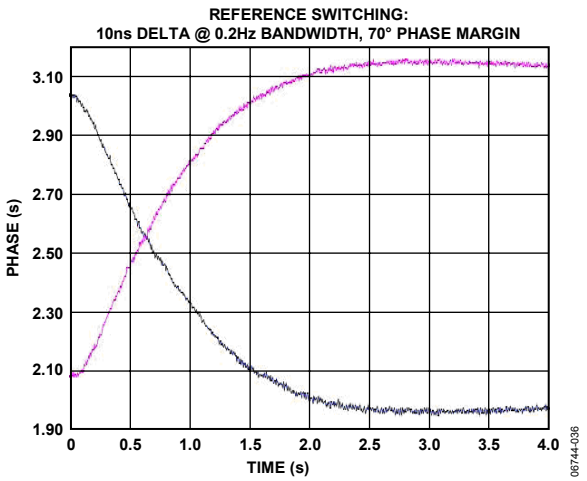


Figure 36. Output Phase vs. Time for a Reference Switchover

Figure 36 shows the output phase as a function of time for a reference switchover event. In this example, Reference A and Reference B are both 30.72 MHz and have a 10 ns (102°) phase offset. The digital PLL loop bandwidth is 0.2 Hz.

The frequency disturbance is the slope of the shift in Figure 36. The maximum slope is 4.75 divisions in one second of time, which gives the following transient frequency error, assuming the output is also 30.72 MHz:

$$m = \frac{\Delta y}{\Delta x} = \frac{4.75 \text{ divs}}{1 \text{ s}} = \frac{105°}{1 \text{ s}} = 0.292 \text{ Hz}$$

The maximum frequency error for this transient is

$$MaxFrequencyError = \frac{0.292 \text{ Hz}}{30.72 \text{ MHz}} = 0.0095 \text{ ppm}$$

In order to apply this to a general case, the designer should calculate the maximum time difference between two reference edges that are 180° apart. The preceding calculation of the slope, m, becomes 0.5 Hz, not 0.292 Hz for a phase shift of 180°. Next, the frequency error must be scaled for the loop bandwidth used. The frequency error for a 1 kHz is 5000 times greater than for 0.2 Hz, so the peak frequency error for the preceding example of 102° is 47.4 ppm, and 81.3 ppm for a 180° phase error between the reference inputs.

When calculating frequency error for a hitless switchover environment, such as Stratum-3 as defined in Telcordia GR-1244-CORE, the designer must consider the frequency error budget for the entire system, and the frequency disturbance caused by a reference clock switchover in the AD9549 contributes to this budget.

It is also critical that the designer differentiate between applications that require the output clock to track the input clock as opposed to applications that require the PLL to smooth out transient disturbances on the input.

Based on all of the preceding considerations, the AD9549 digital PLL architecture allows the designer to choose a loop bandwidth tailored to meet the requirements for a given application. The loop bandwidth can range from 0.1 Hz up to 100 kHz, provided the loop bandwidth is never more than 1/10th of the phase detector frequency.

HOLDOVER

Holdover Control and Frequency Accuracy

Holdover functionality provides the user with a means of maintaining the output clock signal even in the absence of a reference signal at the REFA or REFB input. In holdover mode, the output clock is generated from the SYSCLK input (via the DDS) by directly applying a frequency tuning word to the DDS. The frequency accuracy of the AD9549 is exactly the frequency accuracy of the system clock input.

Transfer from normal operation to holdover mode can be accomplished either manually or automatically by appropriately programming the Automatic Holdover bit (0 = manual, 1 = auto). The actual transfer to holdover operation, however, depends on the state of the HOLDOVER pin and the state of the Enable Holdover Override and Holdover On/Off control register bits.

Manual holdover is established when the Automatic Holdover bit is a Logic 0 (default). In manual mode, holdover is determined by the state of the HOLDOVER pin (0 = normal, 1 = holdover). The HOLDOVER pin is configured as a high impedance (>100 kΩ) input pin in order to accommodate manual holdover operation.

Automatic holdover is invoked when the Automatic Holdover bit is a Logic 1. In automatic mode, the HOLDOVER pin is configured as a low impedance output with its logic state indicating the holdover state as determined by the internal state machine (0 = normal, 1 = holdover).

In automatic holdover operation, the user can override the internal state machine by programming the Enable Holdover Override bit to a Logic 1 and the Holdover Mode bit to the desired state (0 = normal, 1 = holdover). However, the HOLDOVER pin does not indicate the forced holdover state in the override condition but continues to indicate the holdover state as chosen by the internal state machine (even though the state machine choice is overridden). This allows the user to force a holdover state by means of the programming registers while monitoring the response of the state machine via the HOLDOVER pin. A diagram of the reference switchover and holdover logic is shown in Figure 33.

Note that the default state for the reference switchover bits is Automatic Holdover = 0, Enable Holdover Override = 0, and Holdover Mode = 0.

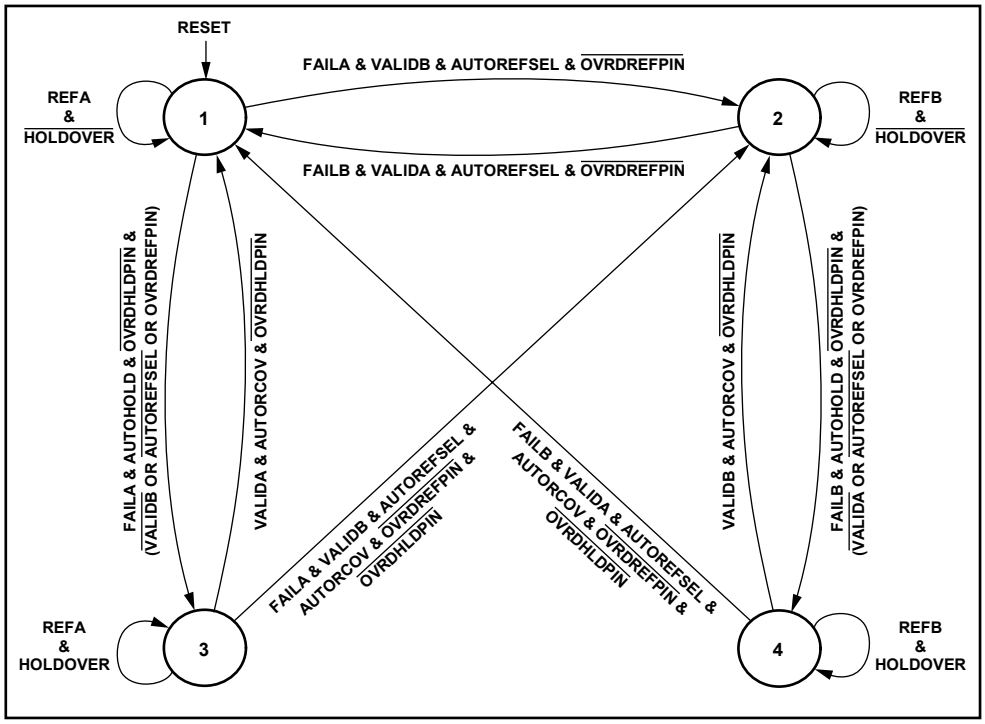
Holdover and Reference Switchover State Machine

The interplay between the input reference signals and holdover is shown in Figure 37. The various control signals and the four states are shown.

State 1 or State 2 is in effect when the device is not in the holdover condition, while State 3 or State 4 is in effect when the holdover condition is active. When REFA is selected as the active reference, then State 1 or State 3 is in effect. When REFB

is selected as the active reference, then State 2 or State 4 is in effect. A transition between states depends on the reference switchover and holdover control register settings, the logic state of the REFSELECT and HOLDOVER pins, and the occurrence of certain events (for example, a reference failure).

The state machine and its relationship to control register and external pin stimuli are shown in Figure 37. The state machine generates a derived reference selection and holdover state. The actual control signal sent to the reference switchover logic and the holdover logic, however, depends on the control signals applied to the muxes. The dashed path leading to the REFSELECT and HOLDOVER pins is active when the auto mode is selected for reference selection and/or holdover assertion.



ABBREVIATION KEY			
REFA:	REFERENCE A SELECTED	OVRDREFPIN:	OVERRIDE REF SEL PIN
REFB:	REFERENCE B SELECTED	OVRDHLDPIN:	OVERRIDE HOLDOVER PIN
HOLDOVER:	HOLDOVER STATE	AUTOREFSEL:	AUTOMATIC REFERENCE SELECT
FAILA:	REFERENCE A FAILED	AUTORCOV:	AUTOMATIC HOLDOVER RECOVERY
FAILB:	REFERENCE B FAILED	AUTOHOLD:	AUTOMATIC HOLDOVER ENTRY
VALIDA:	REFERENCE A VALIDATED	||:	LOGICAL OR
VALIDB:	REFERENCE B VALIDATED	&:	LOGICAL AND
		%:	LOGICAL NOT

06744-037

Figure 37. Holdover State Diagram

Reference Validation Timers

Each of the two reference inputs has a dedicated validation timer. The status of these timers is used by the holdover state machine as part of the decision making process for reverting to a previously faulty reference. For example, suppose that a reference fails (that is, an LOR or OOL condition is in effect) and that the device is programmed to revert automatically to a valid reference when it recovers. When a reference returns to normal operation, the LOR and OOL conditions are no longer true. However, the state machine is not immediately notified of the clearing of the LOR and OOL conditions. Instead, once both the LOR and OOL conditions are cleared, the validation timer for that particular reference is started. Expiration of the validation timer is an indication to the state machine that the reference is now available for selection. However, even though the reference is now flagged as valid, actual transition to the recovered reference depends on the programmed settings of the various holdover control bits.

The validation timers are controlled via the I/O register map. The user should be careful to make sure the validation timer is at least two periods of the reference clock. Although there are two independent validation timers, the programmed information is shared by both. The desired time interval is controlled via a 5-bit word (T) such that $0 \le T \le 31$ (default is T = 0). The duration of the validation timers is given by

$$T_{RECOVER} = T_0\left(2^{T+1} - 1\right)$$

where T_0 is the sample rate of the digital loop filter, whose period is

$$T_0 = \frac{2^{P_{IO}}}{f_S}$$

(See the Digital Loop Filter section.)

Holdover Operation

When the holdover condition is asserted, the DDS output frequency is no longer controlled by the phase lock feedback loop. Instead, a static frequency tuning word (FTW) is applied to the DDS to hold it at a specified frequency. The source of the static FTW depends on the status of the appropriate control register bits. During normal operation, the averager and sampler monitors and accumulates up to 65,000 FTW values as they are generated, and upon entering holdover, the holdover state machine can use the averaged tuning word or the last valid tuning word.

Holdover mode is exited in a similar manner that it is entered. If manual holdover control is used, then when the holdover pin is deasserted, the phase detector starts comparing the holdover signal with the reference input signal and starts to adjust the phase/frequency using the holdover signal as its starting point.

The behavior of the holdover state machine when it is in automatically exiting holdover mode is very similar. The primary difference is that reference monitor is continuously monitoring both reference inputs and, as soon as one becomes valid, it automatically switches to that input.

The output frequency in holdover mode depends on the frequency of the SYSCLK input source and the value of the frequency tuning word applied to the DDS. Therefore, the stability of the output signal is completely dependent on the stability of the SYSCLK source (and the SYSCLK PLL multiplier, if enabled).

Note that it is very important to power down an unused reference input to avoid chattering on that input. In addition, the reference validation timer must be set to at least one full cycle of the signal coming out of the reference divider.

Holdover Sampler and Averager

If activated via the I/O register map, the HSA continuously monitors the data generated by the digital loop filter in the background. It should be noted that the loop filter data is a time sequence of frequency adjustments (Δf) to the DDS. The output of the HSA is routed to a read-only register in the I/O register map and to the holdover control logic.

The first of these destinations (the read-only register) serves as a trace buffer that can be read by the user and the data processed externally. The second destination (the holdover control logic) uses the output of the HSA to peg the DDS at a specific frequency upon entry into the holdover state. Hence, the DDS assumes a frequency specified by the last value generated by the HSA just prior to entering the holdover state.

The state of the output MUX is established by programming the I/O register map. The default state is such that the Δf values pass through the HSA unaltered. In this mode, the output sample rate is f_S/P, the same as the sample rate of the digital loop filter.

Note that P is the divide ratio of the P-divider (see the Digital Loop Filter section), and f_S is the DAC sample rate.

Alternatively, the MUX can be set to select the averaging path. In this mode, a block average is performed on a sequence of samples. The length of the sequence is determined by programming the value of Y (a 4-bit number stored in the I/O register map) and has a value of 2^{Y+1}. In the averaging mode, the output sample rate is given by $f_S/(P \times 2^{Y+1})$.

When the number of Δf samples specified by Y has been collected, the averaged result is delivered to a two-stage pipeline. The last stage of the pipeline contains the value that is delivered to the holdover control logic when a transition into the holdover state occurs. The pipeline is a guarantee that the averaged Δf value delivered to the holdover control logic has not been interrupted by the transition into the holdover state.

The pipeline provides an inherent delay of $\Delta t = P \times 2^{Y+1}/f_S$. Hence, the DDS hold frequency is the average as it appeared Δt to 2Δt seconds prior to entering the holdover state. Note that the user has some control over the duration of Δt because it is dependent on the programmed value of Y.

OUTPUT FREQUENCY RANGE CONTROL

Under normal operating conditions, its output frequency is dynamically changing in response to the output of the digital loop filter. The loop filter can steer the DDS to any frequency between dc and $f_S/2$ (with 48-bit resolution). However, the user is given the option of placing limits on the tuning range of the DDS via two 48-bit registers in the I/O register map: FTW Upper Limit and FTW Lower Limit. If the tuning word input exceeds the upper or lower frequency limit boundaries, the tuning word is clipped to the appropriate value. The default setting for these registers is $f_S/2$ and dc, respectively.

It may be desirable to limit the output range of the DDS to a narrow band of frequencies (for example, to achieve better jitter performance in conjunction with a band pass filter). See the Use of Narrow-Band Filter for High Performance section for more information about this feature.

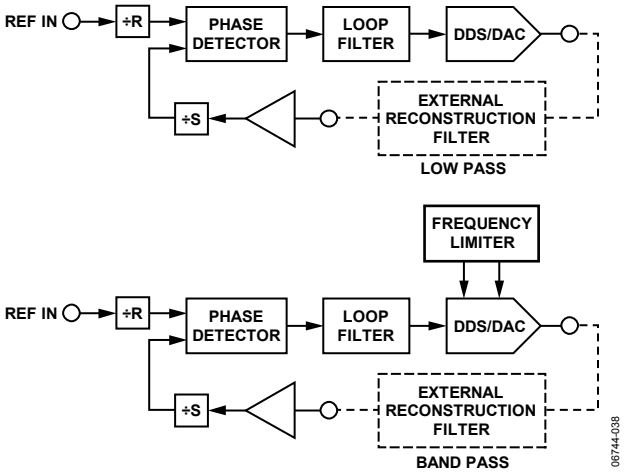


Figure 38. Application of the Frequency Limiter

RECONSTRUCTION FILTER

The origin of the output clock signal produced by the AD9549 is the combined DDS and DAC. The DAC output signal appears as a sinusoid sampled at f_S. The frequency of the sinusoid is determined by the frequency tuning word (FTW) that appears at the input to the DDS. The DAC output is typically passed through an external reconstruction filter that serves to remove the artifacts of the sampling process and other spurs outside the filter bandwidth. The signal is then brought back on-chip to be converted to a square wave that is routed internally to the output clock driver or the 2× DLL multiplier.

Because the DAC constitutes a sampled system, its output must be filtered so that the analog waveform accurately represents the digital samples supplied to the DAC input. The unfiltered DAC output contains the desired baseband signal, which extends from dc to the Nyquist frequency ($f_S/2$). It also contains images of the baseband signal that theoretically extend to infinity. Notice that the odd images (shown in Figure 39) are mirror images of the baseband signal. Furthermore, the entire DAC output spectrum is affected by a sin(x)/x response, which is caused by the sample and hold nature of the DAC output signal.

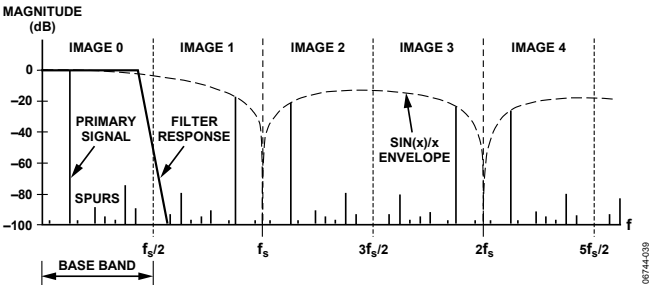


Figure 39. DAC Spectrum vs. Reconstruction Filter Response

The response of the reconstruction filter should preserve the baseband signal (image 0), while completely rejecting all other images. However, a practical filter implementation typically exhibits a relatively flat pass band that covers the desired output frequency plus 20%, roll off as steeply as possible, and then maintain significant (though not complete) rejection of the remaining images.

Because the DAC output signal serves as the feedback signal for the digital PLL, the design of the reconstruction filter can have a significant impact on the overall jitter performance. Hence, good filter design and implementation techniques are important for obtaining the best possible jitter results.

Use of Narrow-Band Filter for High Performance

A distinct advantage of the AD9549 architecture is its ability to constrain the frequency output range of the DDS. This allows the user to employ a narrow-band reconstruction filter instead of the low-pass response shown in Figure 39, resulting in less jitter on the output. For example, suppose that the nominal output frequency of the DDS is 150 MHz. One might then choose a 5 MHz narrow band filter centered at 150 MHz. By using the AD9549's DDS frequency limiting feature, the user can constrain the output frequency to 150 MHz ± 4.9 MHz (which allows for a 100 kHz margin at the pass-band edges). This ensures that a feedback signal is always present for the digital PLL. Such a design is extremely difficult to implement with conventional PLL architectures.

FDBK INPUTS

The FDBK pins serve as the input to the feedback path of the digital PLL. Typically, these pins are used to receive the signal generated by the DDS after it has been band-limited by the external reconstruction filter.

A diagram of the FDBK input pins is provided in Figure 40, which includes some of the internal components used to bias the input circuitry. Note that the FDBK input pins are internally biased to a dc level of ~1 V. Care should be taken to ensure that any external connections do not disturb the dc bias because this may significantly degrade performance.

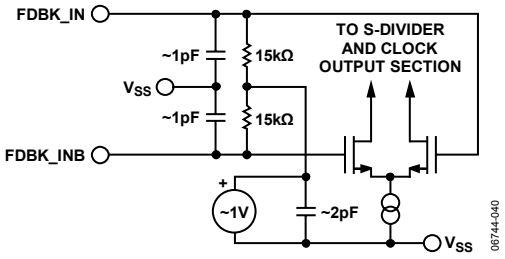


Figure 40. Differential FDBK Inputs

REFERENCE INPUTS

Reference Clock Receiver

The reference clock receiver is the point at which the user supplies the input clock signal that the synchronizer synthesizes into an output clock. The clock receiver circuit is able to handle a relatively broad range of input levels as well as frequencies from 8 kHz up to 750 MHz.

Figure 41 is a diagram of the REFA/REFB input pins, which includes some of the internal components used to bias the input circuitry. Note that the REF input pins are internally biased by a dc source, V_B. Care should be taken to ensure that any external connections do not disturb the dc bias, as this may significantly degrade performance.

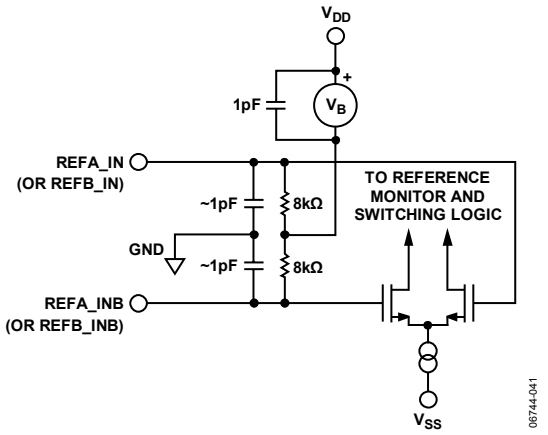


Figure 41. Reference Inputs

Note that support for redundant reference clocks is achieved by using the two reference clock receivers (REFA and REFB).

In order to accommodate a variety of input signal conditions, the value of V_B is programmable via a pair of bits in the I/O register map. Table 5 gives the value of V_B for the bit pattern in Register 040F.

Table 5. Setting of Input Bias Voltage (V_B)

Reference Bias Level Register 040F[1:0]	V_B
00 (default)	AVDD3 – 800 mV
01	AVDD3 – 400 mV
10	AVDD3 – 1600 mV
11	AVDD3 – 1200 mV

SYSCLK INPUTS

Functional Description

The SYSCLK pins are where an external time base is connected to the AD9549 for generating the internal high frequency system clock (f_S).

The SYSCLK inputs can be operated in one of three modes:

- SYSCLK PLL bypassed
- SYSCLK PLL enabled with input signal generated externally
- Crystal resonator with SYSCLK PLL enabled

A functional diagram of the system clock generator is shown in Figure 42.

The SYSCLK PLL multiplier path is enabled by a Logic 0 (default) in the PD SYSCLK PLL location of the I/O register map. The SYSCLK PLL multiplier can be driven from the SYSCLK input pins by one of two means depending on the logic level applied to the 1.8V CMOS CLKMODESEL pin. When CLKMODESEL = 0, a crystal can be connected directly across the SYSCLK pins. When CLKMODESEL = 1, the maintaining amp is disabled, and an external frequency source (oscillator, signal generator, etc.) can be connected directly to the SYSCLK input pins. Note that CLKMODESEL = 1 does not disable the system clock PLL.

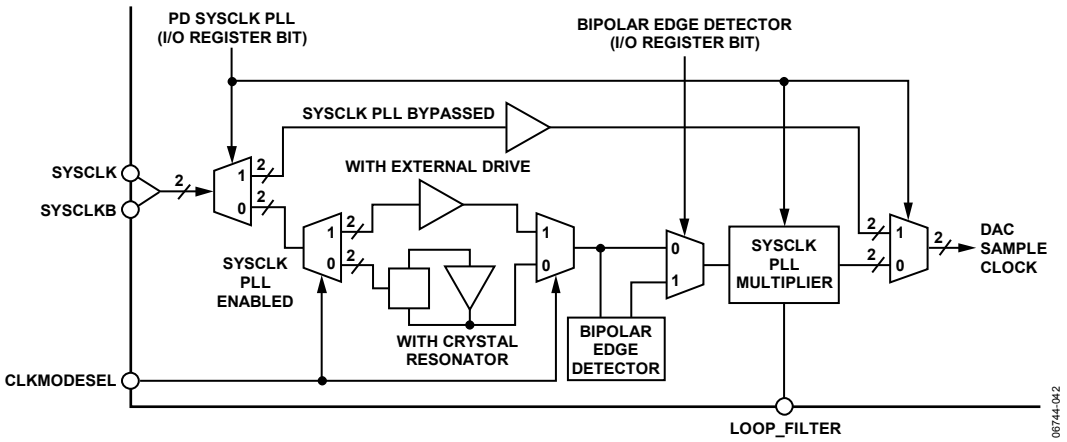


Figure 42. System Clock Generator Block Diagram

The maintaining amp on the AD9549 SYSCLK pins is intended for 25 MHz, 3.2 mm × 2.5 mm AT cut fundamental mode crystals with a maximum motional resistance of 100 Ω. The following crystals, listed in alphabetical order, meet these criteria (as of the revision date of this data sheet):

- AVX/Kyocera CX3225SB
- ECS ECX-32
- Epson/Toyocom TSX-3225
- Fox FX3225BS
- NDK NX3225SA

Note that while these crystals meet the preceding criteria according to their data sheets, Analog Devices, Inc., does not guarantee their operation with the AD9549, nor does Analog Devices endorse one supplier of crystals over another.

When the SYSCLK PLL multiplier path is disabled, the AD9549 must be driven by a high frequency signal source (500 MHz to 1 GHz). The signal thus applied to the SYSCLK input pins becomes the internal DAC sampling clock (f_S) after passing through an internal buffer.

SYSCLK PLL Doubler

The SYSCLK PLL multiplier path offers an optional SYSCLK PLL doubler. This block comes before the SYSCLK PLL multiplier and acts as a frequency doubler by generating a pulse on each edge of the SYSCLK input signal. The SYSCLK PLL multiplier locks to the falling edges of this regenerated signal.

The impetus for doubling the frequency at the input of the SYSCLK PLL multiplier is that an improvement in overall phase noise performance can be realized. The main drawback is that the doubler output is not a rectangular pulse with a constant duty cycle even for a perfectly symmetric SYSCLK input signal. This results in a subharmonic appearing at the same frequency as the SYSCLK input signal, and the magnitude of the subharmonic can be quite large. When employing the doubler, care must be taken to ensure that the loop bandwidth of the SYSCLK PLL multiplier adequately suppresses the subharmonic.

The benefit offered by the doubler depends on the magnitude of the subharmonic, the loop bandwidth of the SYSCLK PLL multiplier, and the overall phase noise requirements of the specific application. In many applications, the AD9549 clock output is applied to the input of another PLL, and the subharmonic is often suppressed by the relatively narrow bandwidth of the downstream PLL.

Note that generally, the benefits of the SYSCLK PLL doubler are realized for SYSCLK input frequencies of 25 MHz and above.

SYSCLK PLL Multiplier

When the SYSCLK PLL m ultiplier path is employed, the frequency applied to the SYSCLK input pins must be limited so as not to exceed the maximum input frequency of the SYSCLK PLL phase detector. A block diagram of the SYSCLK generator appears in Figure 43.

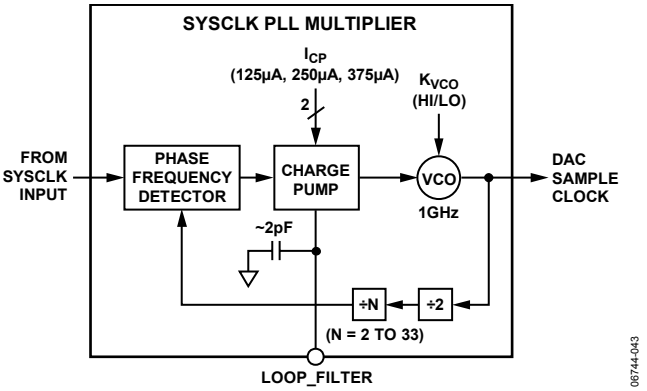


Figure 43. Block Diagram of the SYSCLK PLL

The SYSCLK PLL multiplier has a 1 GHz VCO at its core. A phase/frequency detector (PFD) and charge pump provide the steering signal to the VCO in typical PLL fashion. The PFD operates on the falling edge transitions of the input signal, which means that the loop locks on the negative edges of the reference signal. The charge pump gain is controlled via the I/O register map by selecting one of three possible constant current sources ranging from 125 µA to 375 µA in 125 µA steps. The center frequency of the VCO is also adjustable via the I/O register map and provides high/low gain selection. The feedback path from VCO to PFD consists of a fixed divide-by-2 prescaler followed by a programmable divide-by-N block, where $2 \le N \le 33$. This limits the overall divider range to any even integer from 4 to 66, inclusive. The value of N is programmed via the I/O register map via a 5-bit word that spans a range of 0 to 31, but the internal logic automatically adds a bias of 2 to the value entered, extending the range to 33. Care should be taken when choosing these values so as to not exceed the maximum input frequency of the SYSCLK PLL phase detector or SYSCLK PLL doubler. These values can be found in the AC Specifications section.

External Loop Filter (SYSCLK PLL)

The loop bandwidth of the SYSCLK PLL multiplier can be adjusted by means of three external components as shown in Figure 44. The nominal gain of the VCO is 800 MHz/V. The recommended component values are shown in Table 6. They establish a loop bandwidth of approximately 1.6 MHz with the charge pump current set to 250 µA. The default case is N = 40 and assumes a 25 MHz SYSCLK input frequency and generates an internal DAC sampling frequency (f_S) of 1 GHz.

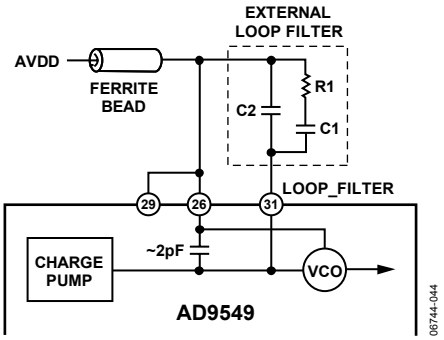


Figure 44. External Loop Filter for SYSCLK PLL

Table 6: Recommended Loop Filter Values for a Nominal 1.5 MHz SYSCLK PLL Loop Bandwidth

Multiplier	R1	Series C1	Shunt C2
<8	390 Ω	1 nF	82 pF
10	470 Ω	820 pF	56 pF
20	1 kΩ	390 pF	27 pF
40 (default)	2.2 kΩ	180 pF	10 pF
60	2.7 kΩ	120 pF	5 pF

Detail of SYSCLK Differential Inputs

A diagram of the SYSCLK input pins is provided in Figure 45. Included are details of the internal components used to bias the input circuitry. These components have a direct effect on the static levels at the SYSCLK input pins. This information is intended to aid in determining how best to interface to the device for a given application.

Note that the SYSCLK PLL bypassed and SYSCLK PLL enabled input paths are internally biased to a dc level of ~1 V. Care should be taken to ensure that any external connections do not disturb the dc bias because this may significantly degrade performance. Generally, it is recommended that the SYSCLK inputs be ac-coupled to the signal source (except when using a crystal resonator).

HARMONIC SPUR REDUCTION

The most significant spurious signals produced by the DDS are harmonically related to the desired output frequency of the DDS. The source of these harmonic spurs can usually be traced to the DAC, and the spur level is in the −60 dBc range. This ratio represents a level that is about 10 bits below the full-scale output of the DAC (10 bits down is 2^{-10}, or 1/1024).

To reduce such a spur requires combining the original signal with a replica of the spur but offset in phase by 180°. This idea is the foundation of the technique used to reduce harmonic spurs in the AD9549. Because the DAC has 14-bit resolution, a −60 dBc spur can be synthesized using only the lower 4 bits of the DAC full-scale range. That is, the 4 LSBs can create an output level approximately 60 dB below the full-scale level of the DAC (commensurate with a −60 dBc spur). This fact gives rise to a means of digitally reducing harmonic spurs or their aliased images in the DAC output spectrum by digitally adding a sinusoid at the input of the DAC with similar magnitude as the offending spur but shifted in phase to produce destructive interference.

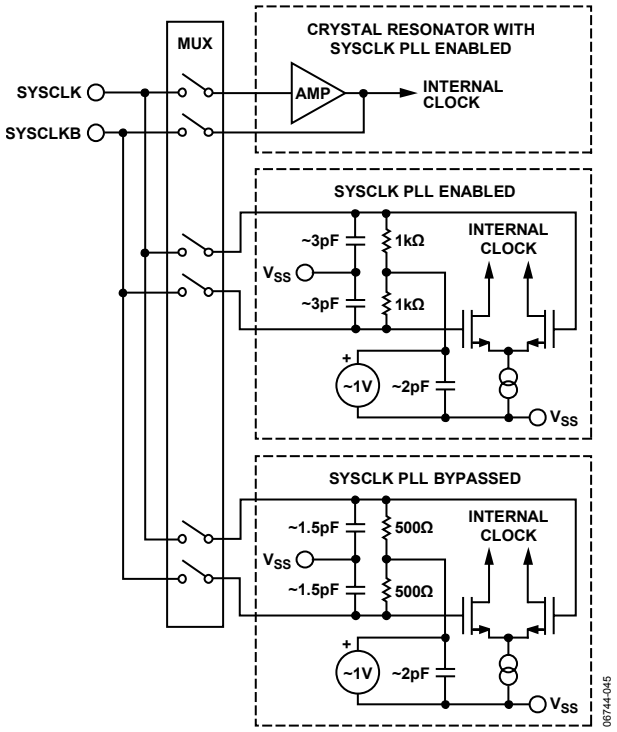


Figure 45. Differential SYSCLK Inputs

Although the worst spurs tend to be harmonic in origin, the fact that the DAC is part of a sampled system results in the possibility of some harmonic spurs appearing in nonharmonic locations in the output spectrum. For example, if the DAC is sampled at 1 GHz and generates an output sinusoid of 170 MHz, the 5th harmonic would normally be at 850 MHz. However, because of the sampling process, this spur appears at 150 MHz, only 20 MHz away from the fundamental. Hence, when attempting to reduce DAC spurs it is important to know the actual location of the harmonic spur in the DAC output spectrum based on the DAC sample rate so that its harmonic number can be reduced.

The mechanics of performing harmonic spur reduction is shown in Figure 46. It essentially consists of two additional DDS cores operating in parallel with the original DDS. This enables the user to reduce two different harmonic spurs from the 2nd to the 15th with 9 bits of phase offset control (±π) and 8 bits of amplitude control.

The dynamic range of the cancellation signal is further augmented by a gain bit associated with each channel. When this bit is set, the magnitude of the cancellation signal is doubled by employing a 1-bit left-shift of the data. However, the shift operation reduces the granularity of the cancellation signal magnitude.

Note that the full-scale amplitude of a cancellation spur is approximately −60 dBc when the gain bit is a Logic 0 and approximately −54 dBc when the gain bit is a Logic 1.

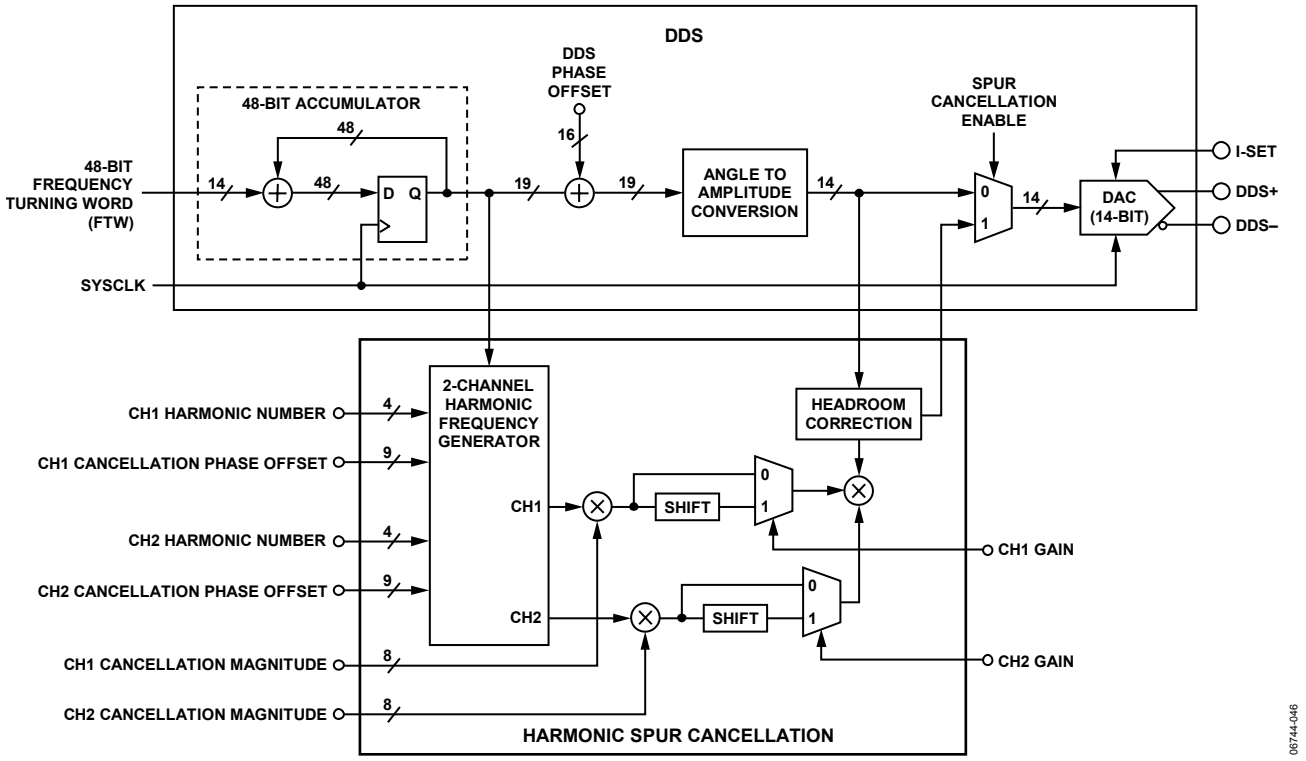


Figure 46. Spur Reduction Technique

OUTPUT CLOCK DRIVERS AND 2× FREQUENCY MULTIPLIER

There are two output drivers provided by the AD9549. The primary supports differential 1.8 V HSTL output levels while the secondary supports either 1.8 V or 3.3 V CMOS levels, depending on whether Pin 37 is driven at 1.8 V or 3.3 V.

The primary differential driver nominally provides an output voltage with 100 Ω load applied differentially ($V_{DD} - V_{SS}$ = 1.8 V). The source impedance of the driver is approximately 100 Ω for most of the output clock period; during transition between levels, the source impedance reaches a maximum of about 500 Ω. The driver is designed to support output frequencies of up to and beyond the OC-12 network rate of 622.08 MHz.

The output clock can also be powered down by a control bit in the I/O register map.

Primary 1.8 V Differential HSTL Driver

The DDS produces a sinusoidal clock signal that is sampled at the system clock rate. This DDS output signal is routed off-chip where it is passed through an analog filter and brought back on-chip for buffering and, if necessary, frequency doubling. Where possible, for the best jitter performance, it is recommended that the upconverter be bypassed.

The 1.8 V HSTL output driver should be ac-coupled, with 100 Ω termination at the destination. The driver design has low jitter injection for frequencies in the range of 50 MHz to 750 MHz. Refer to the AC Specifications section for the exact frequency limits.

2× Frequency Multiplier

The AD9549 can be configured (via the I/O register map) with an internal 2× delay-locked loop (DLL) multiplier at the input of the primary clock driver. The extra octave of frequency gain allows the AD9549 to provide output clock frequencies that exceed the range available from the DDS alone. These settings are found in Register 0010 and Register 0200.

The input to the DLL consists of the filtered DDS output signal after it has been squared up by an integrated clock receiver circuit. The DLL can accept input frequencies in the range of 200 MHz to 400 MHz.

Single-Ended CMOS Output

In addition to the high speed differential output clock driver, the AD9549 provides an independent, single-ended output, CMOS clock driver. It serves as a relatively low speed (<150 MHz) clock source. The origin of the signal generated by the CMOS clock driver is determined by the appropriate control bits in the I/O register map. The user can select one of two sources under program control.

One source is the signal generated by the DDS after it has been externally filtered and brought back on-chip. In this configuration, the CMOS clock driver generates the same frequency as appears at the output of the DDS.

Note that in this configuration, the DDS output frequency must not exceed 50 MHz.

The other source is the output of the feedback divider (S-divider). In this configuration, the CMOS clock driver generates the same frequency as the input reference after optional prescaling by the R-divider (that is, $f_{CMOS} = f_R/R$), which is inherently limited to a maximum of 25 MHz.

FREQUENCY SLEW LIMITER

The AD9549 offers frequency slew limiting capability enabling users to specify the maximum rate of frequency change that appears at the output. The function is programmable via the I/O register map. Program control a bit to enable/disable the function (default condition is disable) and a register that sets the desired slew rate.

The frequency slew limiter is located between the digital loop filter and the CCI filter, as shown in Figure 47.

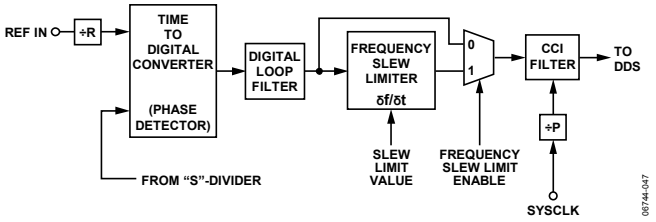


Figure 47. Frequency Slew Limiter

The frequency slew limiter sets a boundary on the rate of change of the output frequency of the DDS. The frequency slew limiting constant, K_{SLEW}, is a 48-bit value stored in the I/O register map. The value of the constant is determined by

$$K_{SLEW} = \text{round}\left[\left(\frac{2^{48+P_{IO}}}{{f_S}^2}\right)\frac{\delta f}{\delta t}\right]$$

where:
P_{IO} is the value stored in the I/O register map for the P-divider.
f_S is the DAC sample rate.
$\delta f/\delta t$ is the desired frequency slew rate limitation.

For example, suppose that f_S = 1 GHz, P_{IO} = 9, and $\delta f/\delta t$ = 5 kHz/second, then

$$K_{SLEW} = \text{round}\left[\left(\frac{2^{48+9}}{(10^9)^2}\right)\left(5\times 10^3\right)\right] = 721$$

The resulting slew rate can be calculated as

$$\frac{\delta f}{\delta t} = K_{SLEW}\left(\frac{{f_S}^2}{2^{48+P_{IO}}}\right)$$

The preceding example yields $\delta f/\delta t$ = 5.003 kHz/s.

FREQUENCY ESTIMATOR

The AD9549 has a frequency estimation function that automatically sets the DDS output frequency so that the feedback frequency (f_{DDS}/S) and the prescaled reference frequency (f_{REF_IN}/R) are matched within an error tolerance (ε_0). Its primary purpose is to allow the PLL to quickly lock when the reference frequency is not known. The error tolerance is defined as a fractional error and is controlled by a 16-bit programmable value (K) via the I/O register map.

The precision of any frequency measurement is dependent on two factors:

- The timing resolution of the measurement device (δt)
- The duration of the measurement (T_{meas})

The frequency estimator uses f_S as its measurement reference, so $\delta t = 1/f_S$ (that is, δt = 1 ns for a 1 GHz DAC sample rate). The duration of the measurement is controlled by K, which establishes a measurement interval that is K cycles of the measured signal such that $T_{meas} = KR/f_{REF\_IN}$.

The frequency estimator uses a 17-bit counter to accumulate the number of δt periods within the measurement interval. The finite capacity of the counter puts an upper limit on the duration of the measurement, which is constrained to $T_{max} = 2^{17}/f_S$. If f_S = 1 GHz, then this equates to ~131 µs. The fact that the measurement time is bounded by T_{max} means there is a limit to the largest value of K (K_{MAX}) that can be used without causing the counter to overflow. The value of K_{MAX} is given by

$$K_{MAX} = floor\left(\frac{65{,}535}{\rho}\right)$$

where:

$$\rho = \frac{f_S R}{f_R}$$

R is the modulus of the feedforward divider.
f_R is the input reference frequency.

The measurement error (ε) associated with the frequency estimator depends on the choice of the measurement interval parameter (K). These are related by

$$\varepsilon = \frac{\rho K}{\text{floor}(\rho K) - 1} - 1$$

With a specified fractional error (ε_0), only those values of K for which $\varepsilon \le \varepsilon_0$ results in a frequency estimate that meets the requirements. A plot of ε vs. K (for a given ρ) takes on the general form shown in Figure 48.

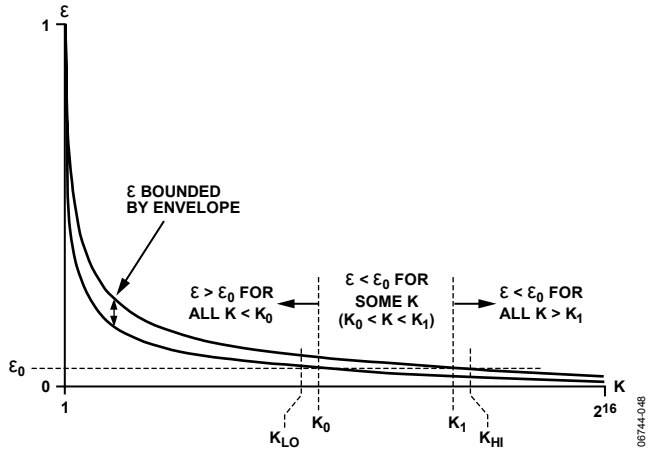


Figure 48. Frequency Estimator ε vs. K

An iterative technique is necessary to determine the exact values of K_0 and K_1. However, a closed form exists for a conservative estimate of K_0 (K_{LO}) and K_1 (K_{HI}).

$$K_{LO} = \text{ceil}\left[\frac{1}{\rho}\left(1+\frac{1}{\varepsilon_0}\right)\right]$$

$$K_{HI} = \text{ceil}\left[\frac{2}{\rho}\left(1+\frac{1}{\varepsilon_0}\right)\right]$$

As an example, consider the following system conditions:

f_S = 400MHz
R = 8
f_{REF_IN} = 155.52 MHz
ε_0 = 0.00005 (that is, 50 ppm)

These conditions yield K_{MAX} = 3185, which is the largest K value that can be programmed without causing the frequency estimator counter to overflow. With K = K_{MAX}, T_{meas} = 163.84 µs, and ε = 30.2 ppm, K_{MAX} generally (but not always) yields the smallest value of ε, but this comes at the cost of the largest measurement time (T_{meas}).

If the measurement time must be reduced, then K_{HI} can be used instead of K_{MAX}. This yields K_{HI} = 1945, T_{meas} = 100.05 µs, and ε = 39.4 ppm.

The measurement time can be further reduced (though marginally) by using K_1 instead of K_{HI}. K_1 is found by solving the $\varepsilon \le \varepsilon_0$ inequality iteratively. To do so, start with K = K_{HI} and decrement K successively while evaluating the inequality for each value of K. Stop the process the first time that the inequality is no longer satisfied and add 1 to the value of K thus obtained. The result is the value of K_1. For the preceding example, K_1 = 1912, T_{meas} = 98.35 µs, and ε = 39.8 ppm.

If a further reduction of the measurement time is necessary, then K_0 can be used. K_0 is found in a manner similar to K_1. Start with K = K_{LO} and increment K successively while evaluating the inequality for each value of K. Stop the process the first time that the inequality is satisfied. The result is the value of K_0. For the preceding example, K_0 = 1005, T_{meas} = 51.70 µs, and ε = 49.0 ppm.

STATUS AND WARNINGS

Status Pins

Four pins (S1 to S4) are reserved for providing device status information to the external environment. These four pins are individually programmable (via the serial I/O port) as an OR'ed combination of six possible status indications. Each pin has a dedicated group of control register bits that determine which internal status flags are used to provide an indication on a particular pin (as shown in Figure 49).

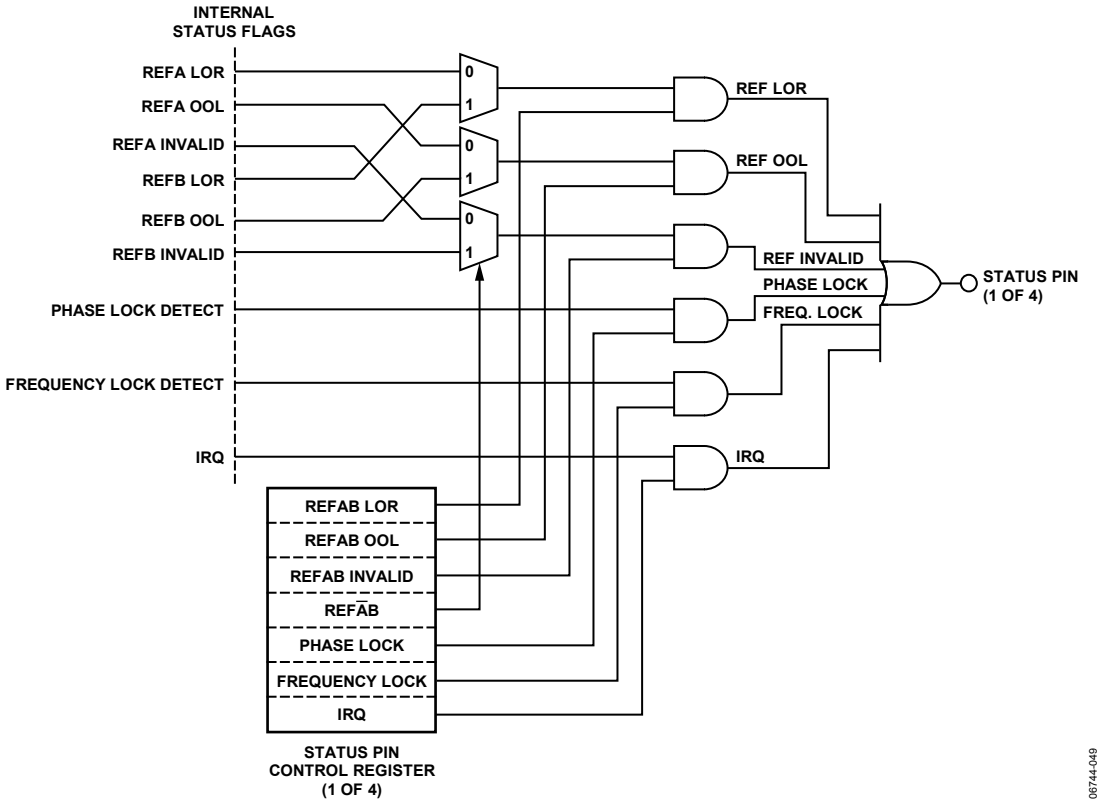


Figure 49. Status Pin Control

Reference Monitor Status

In the case of reference monitoring status information, a pin can be programmed for either REFA or REFB, but not both. In addition, the OR'ed output configuration allows the user to combine multiple status flags into a single status indication. For example, if both the LOR and OOL control register bits are true, the status pin associated with that particular control register gives an indication if either the LOR or OOL status flag is asserted for the selected reference (A or B).

Default DDS Output Frequency on Power-Up

The four status pins (S1 to S4) provide a completely separate function at power-up. They can be used to define the output frequency of the DDS at power-up even though the I/O registers have not yet been programmed. This is made possible because the status pins are designed with bidirectional drivers. At power-up, internal logic initiates a reset pulse of about 10 ns. During this time, S1 to S4 briefly function as input pins and can be driven externally. Any logic levels thus applied are transferred to a 4-bit register on the falling edge of the internally initiated pulse. The falling edge of the pulse also returns S1 to S4 to their normal function as output pins. The same behavior occurs when the RESET pin is asserted manually.

Setting up S1 to S4 for default DDS start-up is accomplished by connecting a resistor to each pin (either pull-up or pull-down) to produce the desired bit pattern, yielding 16 possible states that are used both to address an internal 8 × 16 ROM and to select the SYSCLK mode (see Table 7). The ROM contains eight 16-bit DDS frequency tuning words (FTWs), one of which is selected by the state of the S1 to S3 pins. The selected FTW is transferred to the FTW0 register in the I/O register map without the need for an I/O update. This ensures that the DDS generates the selected frequency even if the I/O registers have not been programmed. The state of the S4 pin selects whether the internal system clock is generated by means of the internal SYSCLK PLL multiplier or not (see the SYSCLK Inputs section for details).

The DDS output frequency listed in Table 7 assumes that the internal DAC sampling frequency (f_S) is 1 GHz. These frequencies scale 1:1 with f_S, meaning that other startup frequencies are available by varying the SYSCLK frequency.

At startup, the internal frequency multiplier defaults to 40× when the Xtal/PLL mode is selected via the status pins.

Note that when using this mode, the digital PLL loop is still open, and the AD9549 is acting as a frequency synthesizer. The frequency dividers and DPLL loop filter must still be programmed before closing the loop.

Table 7. Default Power-Up Frequency Options for 1 GHz System Clock

Status Pin				SYSCLK Input Mode	Output Frequency (MHz)
S4	S3	S2	S1		
0	0	0	0	Xtal/PLL	0
0	0	0	1	Xtal /PLL	38.87939
0	0	1	0	Xtal /PLL	51.83411
0	0	1	1	Xtal /PLL	61.43188
0	1	0	0	Xtal /PLL	77.75879
0	1	0	1	Xtal /PLL	92.14783
0	1	1	0	Xtal /PLL	122.87903
0	1	1	1	Xtal /PLL	155.51758
1	0	0	0	Direct	0
1	0	0	1	Direct	38.87939
1	0	1	0	Direct	51.83411
1	0	1	1	Direct	61.43188
1	1	0	0	Direct	77.75879
1	1	0	1	Direct	92.14783
1	1	1	0	Direct	122.87903
1	1	1	1	Direct	155.51758

Interrupt Request (IRQ)

Any one of the four status pins (S1 to S4) can be programmed as an IRQ pin. If a status pin is programmed as an IRQ pin, then the state of the internal IRQ flag appears on that pin. An IRQ flag is internally generated based on the change of state of any one of the internal status flags. The individual status flags are routed to a read-only I/O register (Status register) so that the user can interrogate the status of any of these flags at any time. Furthermore, each status flag is monitored for a change in state. In some cases, only a change of state in one direction is necessary (for example, the frequency estimate done flag), but in most cases, the status flags are monitored for a change of state in either direction (see Figure 50).

Whether or not a particular state change is allowed to generate an IRQ is dependent on the state of the bits in the IRQ Mask register. The user programs the mask to enable those events, which are to constitute cause for an IRQ. If an unmasked event occurs, it triggers the IRQ latch and the IRQ flag is asserted (active high). The state of the IRQ flag is made available externally via one of the programmable status pins (see the Status Pins section).

The automatic assertion of the IRQ flag causes the contents of the Status register to be transferred to the IRQ register. The user can then read the IRQ register any time after the indication of an IRQ event (that is, assertion of the IRQ flag). By noting the bits in the IRQ register that is set, the cause of the IRQ event can be determined.

Once the IRQ register has been read, the user must set the IRQ Reset bit in the appropriate control register via the serial I/O port. This restores the IRQ flag to its default state, clears the IRQ status register, and resets the edge detection logic that monitors the status flags in preparation for the next state change.

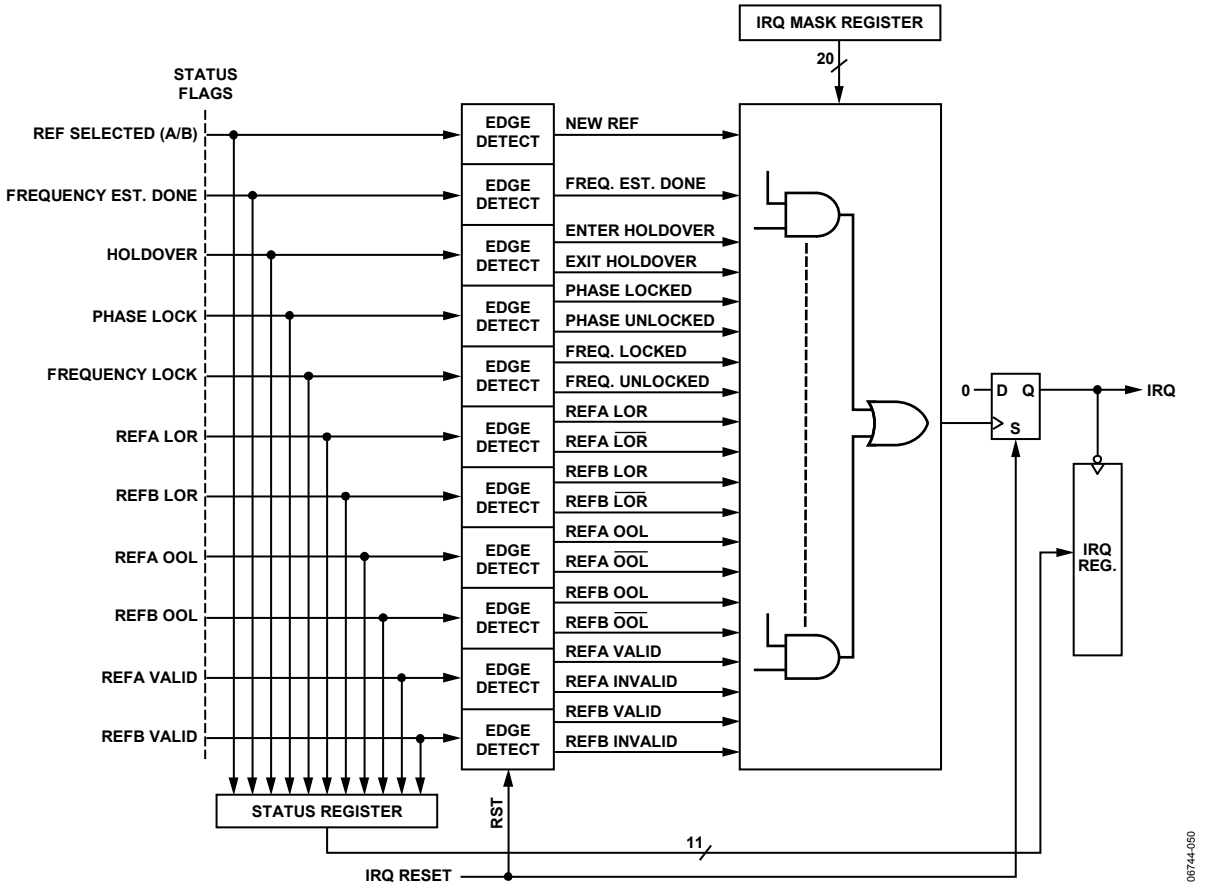


Figure 50. Interrupt Request Logic

THERMAL PERFORMANCE

Table 8. Thermal Parameters for AD9549 64-Lead LFCSP Package

Symbol	Thermal Characteristic Using a JEDEC51-7 Plus JEDEC51-5 2S2P Test Board	Value	Unit
θ_{JA}	Junction-to-ambient thermal resistance, 0.0 m/s air flow per JEDEC JESD51-2 (still air)	25.2	°C/W
θ_{JMA}	Junction-to-ambient thermal resistance, 1.0 m/s air flow per JEDEC JESD51-6 (moving air)	22.0	°C/W
θ_{JMA}	Junction-to-ambient thermal resistance, 2.0 m/s air flow per JEDEC JESD51-6 (moving air)	19.8	°C/W
θ_{JB}	Junction-to-board thermal resistance, 1.0 m/s air flow per JEDEC JESD51-8 (moving air)	13.9	°C/W
θ_{JC}	Junction-to-case thermal resistance (die-to-heat sink) per MIL-Std 883, Method 1012.1	1.7	°C/W
Ψ_{JT}	Junction-to-top-of-package characterization parameter, 0 m/s air flow per JEDEC JESD51-2 (still air)	0.1	°C/W

The AD9549 is specified for a case temperature (T_{CASE}). To ensure that T_{CASE} is not exceeded, an airflow source can be used.

Use the following equation to determine the junction temperature on the application PCB:

$$T_J = T_{CASE} + (\Psi_{JT} \times PD)$$

where:
T_J = junction temperature (°C).
T_{CASE} = case temperature (°C) measured by customer at top center of package.
Ψ_{JT} = value from Table 8.
PD = power dissipation (see the Total Power Dissipation section in the Specifications section)

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first-order approximation of TJ by the equation

$$T_J = T_A + (\theta_{JA} \times PD)$$

where T_A is the ambient temperature (°C).

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heat sink is required.

Values of θ_{JB} are provided for package comparison and PCB design considerations.

AD9549 POWER-UP

POWER-ON RESET

On initial power-up, the AD9549 internally generates a 75 ns RESET pulse. The pulse is initiated when both of the following two conditions are met:

- The 3.3 V supply is greater than 2.35 ± 0.1 V.
- The 1.8 V supply is greater than 1.4 ± 0.05 V.

Less than 1 ns after RESET goes high, the S1 to S4 configuration pins go high impedance and remain high impedance until RESET is deactivated. This allows strapping and configuration during RESET.

Because of this reset sequence, external power supply sequencing is not critical.

PROGRAMMING SEQUENCE

The following sequence should be followed when initializing the AD9549:

1. Apply power. The AD9549 will perform an internal reset.
2. Important: Make sure the desired configuration registers have single tone mode (Register 0100[5]) set, and the Close Loop bit (Register 0100[0]) cleared. If the Close Loop bit is set on initial loading, the AD9549 will attempt to lock the loop before it has been configured.
3. Once the registered are loaded, the OOL (out of limits) and LOR (loss of reference) can be monitored to insure that a valid reference signal is present on REFA or REFB.
4. If a valid reference is present, Register 0100 can be reprogrammed to clear single tone mode and lock the loop.
5. Automatic holdover mode can now be used to make the AD9549 immune to any disturbance on the reference inputs.

The following sequence should be followed when changing frequencies the AD9549:

1. Open the loop and enter single tone mode via Register 0100.
2. Enter the new register settings.
3. Write 0x1E to Register 0012.
4. Once the registered are loaded, the OOL (out of limits) and LOR (loss of reference) can be monitored to insure that a valid reference signal is present on REFA or REFB.
5. If a valid reference is present, Register 0100 can be reprogrammed to clear single tone mode and lock the loop.
6. Automatic holdover mode can now be used to make the AD9549 immune to any disturbance on the reference inputs.

Notes:

- Attempting to lock the loop without a valid reference can put the AD9549 into a state that requires a reset, or at a minimum, writing 0xFF to Register 0012
- Automatic holdover mode is not available unless the loop has been successfully closed.
- If the user desires to open and close the loop manually, writing 0x1E to Register 0012 prior to closing the loop again is recommended.

POWER SUPPLY PARTITIONING

The AD9549 features multiple power supplies, and their power consumption varies with its configuration. This section covers which power supplies can be grouped together and how each block's power consumption varies with frequency.

The numbers quoted here are for comparison only. Please refer to the Specifications section for exact numbers. With each group, bypass caps of 1 µF in parallel with a 10 µF should be used.

The recommendations here are for typical applications, and for these applications, there are four groups of power supplies: 3.3 V digital, 3.3 V analog, 1.8 V digital, and 1.8 V analog.

Applications demanding the highest performance may require additional power supply isolation.

3.3 V SUPPLIES

DVDD_I/O (Pin 1) and AVDD3 (Pin 14): These two 3.3 V supplies can be grouped together. The power consumption on Pin 1 varies dynamically with serial port activity. Noise from the serial port that couples into the reference input should be filtered by the digital PLL.

AVDD3 (Pin 37): This is the CMOS driver supply and can be either 1.8 V or 3.3 V, and its power consumption is a function of the output frequency and loading of OUT_CMOS (Pin 38).

If the CMOS driver is used at 3.3 V, this supply should be isolated from other 3.3 V supplies with a ferrite bead to avoid a spur at the output frequency. If the HSTL driver is not used, AVDD3 (Pin 37) can be connected (using a ferrite bead) to AVDD3 (Pin 46, Pin 47, Pin 49). If the HSTL driver is used, connect AVDD3 (Pin 37) using a ferrite bead to Pin 1 and Pin 14.

If the CMOS driver is used at 1.8 V, AVDD3 (Pin 37) can be connected to AVDD (Pin 36).

If the CMOS driver is not used, AVDD3 (Pin 37) can be tied directly to the 1.8 V AVDD (Pin 36) and the CMOS driver powered down using Register 0010.

AVDD3 (Pin 46, Pin 47, Pin 49): These are 3.3 V DAC power supplies that typically consume about 25 mA. At a minimum, a ferrite bead should be used to isolate these from other 3.3 V supplies, with a separate regulator being ideal.

1.8 V SUPPLIES

DVDD (Pin 3, Pin 5, Pin 7): These pins can be grouped together. Their current consumption increases from about 160 mA at a system clock of 700 MHz to about 220 mA a system clock of 1 GHz. There is also a slight (~5%) increase as f_{OUT} increases from 50 MHz to 400 MHz.

AVDD (Pin 53): This 1.8 V supply consumes about 20 mA to 40 mA. The supply can be run off the same regulator as Pin 3, Pin 5, Pin 7, with a ferrite bead to isolate
Pin 53 from Pin 3, Pin 5, Pin 7.

AVDD (Pin 11, Pin 19, Pin 23, Pin 24, Pin 36, Pin 42, Pin 45): These pins can be grouped together and should be isolated from other 1.8 V supplies. At a minimum, a ferrite bead should be used for isolation, with a separate regulator being ideal.

AVDD (Pin 25, Pin 26, Pin 29, Pin 30): These system clock PLL power pins can be grouped together and should be isolated from other 1.8 V supplies. For most applications, it is recommended to tie Pin 25 and Pin 30 together and to isolate them from their 1.8 V supply with a ferrite bead. Likewise, Pin 26 and Pin 29 can also be tied together, with a ferrite bead isolating them from the same 1.8 V supply. The loop filter for the system clock PLL should connect to Pin 26 and Pin 29.

If the system clock PLL is bypassed, these pins should still be powered, but isolation is not critical.

SERIAL CONTROL PORT

The AD9549 serial control port is a flexible, synchronous, serial communications port that allows an easy interface with many industry-standard microcontrollers and microprocessors. Single or multiple byte transfers are supported, as well as MSB first or LSB first transfer formats. The AD9549 serial control port can be configured for a single bidirectional I/O pin (SDIO only) or for two unidirectional I/O pins (SDIO/SDO).

SERIAL CONTROL PORT PIN DESCRIPTIONS

SCLK (serial clock) is the serial shift clock. This pin is an input. SCLK is used to synchronize serial control port reads and writes. Write data bits are registered on the rising edge of this clock, and read data bits are registered on the falling edge. This pin is internally pulled down by a 30 kΩ resistor to ground.

SDIO (serial data input/output) is a dual-purpose pin and acts as input only or input/output. The AD9549 defaults to bidirectional pins for I/O. Alternatively, SDIO can be used as a unidirectional I/O pin by writing to the SDO Active register at Register 0000[7] = 1. In this case, SDIO is the input, and SDO is the output.

SDO (serial data out) is used only in the unidirectional I/O mode (Register 0000[7] = 1) as a separate output pin for reading back data. Bidirectional I/O mode (using SDIO as both input and output) is active by default (SDO enable register at Register 0000[7] = 0).

CSB (chip select bar) is an active low control that gates the read and write cycles. When CSB is high, SDO and SDIO are in a high impedance state. This pin is internally pulled up by a 100 kΩ resistor to 3.3 V. It should not be left floating. See the Operation of Serial Control Port section on the use of the CSB in a communication cycle.

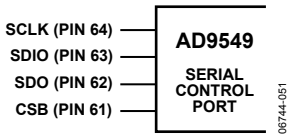


Figure 51. Serial Control Port

OPERATION OF SERIAL CONTROL PORT

Framing a Communication Cycle with CSB

A communication cycle (a write or a read operation) is gated by the CSB line. CSB must be brought low to initiate a communication cycle.

CSB stall high is supported in modes where three or fewer bytes of data (plus instruction data) are transferred (W1:W0 must be set to 00, 01, or 10; see Table 9). In these modes, CSB can temporarily return high on any byte boundary, allowing time for the system controller to process the next byte. CSB can go high on byte boundaries only and can go high during either part (instruction or data) of the transfer. During this period, the serial control port state machine enters a wait state until all data has been sent. If the system controller decides to abort the transfer before all of the data is sent, the state machine must be reset by either completing the remaining transfer or by returning the CSB low for at least one complete SCLK cycle (but fewer than eight SCLK cycles). Raising the CSB on a non-byte boundary terminates the serial transfer and flushes the buffer.

In the streaming mode (W1:W0 = 11), any number of data bytes can be transferred in a continuous stream. The register address is automatically incremented or decremented (see the MSB/LSB First Transfers section). CSB must be raised at the end of the last byte to be transferred, thereby ending the stream mode.

Communication Cycle—Instruction Plus Data

There are two parts to a communication cycle with the AD9549. The first writes a 16-bit instruction word into the AD9549, coincident with the first 16 SCLK rising edges. The instruction word provides the AD9549 serial control port with information regarding the data transfer, which is the second part of the communication cycle. The instruction word defines whether the upcoming data transfer is a read or a write, the number of bytes in the data transfer, and the starting register address for the first byte of the data transfer.

Write

If the instruction word is for a write operation (I15 = 0), the second part is the transfer of data into the serial control port buffer of the AD9549. The length of the transfer (1, 2, 3 bytes, or streaming mode) is indicated by 2 bits (W1:W0) in the instruction byte. The length of the transfer indicated by (W1:W0) does not include the two-byte instruction. CSB can be raised after each sequence of 8 bits to stall the bus (except after the last byte, where it ends the cycle). When the bus is stalled, the serial transfer resumes when CSB is lowered. Stalling on non-byte boundaries resets the serial control port.

There are three types of registers on the AD9549: buffered, live, and read-only. Buffered (also referred to as mirrored) registers require an I/O update to transfer the new values from a temporary buffer on the chip to the actual register and are marked with an M in the column labeled Type of the register map. Toggling the IO_UPDATE pin or writing a 1 to the Register Update bit (Register 0005[0]) causes the update to occur. Because any number of bytes of data can be changed before issuing an update command, the update simultaneously enables all register changes since any previous update. Live registers do not require I/O update and update immediately after being written. Read-only registers ignore write commands and are marked RO in the Type column of the register map. The Type column of the register map may also have an AC, which indicates that the register is auto-clearing.

Read

If the instruction word is for a read operation (I15 = 1), the next N × 8 SCLK cycles clock out the data from the address specified in the instruction word, where N is 1, 2, 3, 4 as determined by W1:W0. In this case, 4 is used for streaming mode where 4 or more words are transferred per read. The data readback is valid on the falling edge of SCLK.

The default mode of the AD9549 serial control port is bidirectional mode, and the data readback appears on the SDIO pin. It is possible to set the AD9549 to unidirectional mode by writing the SDO enable register at Register 0000[7] = 0, and in that mode, the requested data appears on the SDO pin.

By default, a read request reads the register value that is currently in use by the AD9549. However, setting Register 0004[0] = 1 causes the buffered registers to be read instead. The buffered registers are the ones that take effect during the next I/O update.

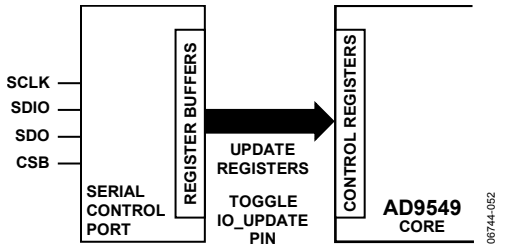


Figure 52. Relationship Between Serial Control Port Register Buffers and Control Registers of the AD9549

The AD9549 uses Register 0000 to Register 0509. Although the AD9549 serial control port allows both 8-bit and 16-bit instructions, the 8-bit instruction mode provides access to five address bits (A4 to A0) only, which restricts its use to the address space 0x00 to 0x01. The AD9549 defaults to 16-bit instruction mode on power-up, and the 8-bit instruction mode is not supported.

THE INSTRUCTION WORD (16 BITS)

The MSB of the instruction word is R/$\overline{W}$, which indicates whether the instruction is a read or a write. The next two bits, W1:W0, are the transfer length in bytes. The final 13 bits are the address (A12:A0) at which to begin the read or write operation.

For a write, the instruction word is followed by the number of bytes of data indicated by Bits W1:W0, which is interpreted according to Table 9.

Bits [A12:A0] select the address within the register map that is written to or read from during the data transfer portion of the communications cycle. The AD9549 uses all of the 13-bit address space. For multibyte transfers, this address is the starting byte address.

Table 9. Byte Transfer Count

W1	W0	Bytes to Transfer (Excluding the 2-Byte Instruction)
0	0	1
0	1	2
1	0	3
1	1	Streaming mode

MSB/LSB FIRST TRANSFERS

The AD9549 instruction word and byte data may be MSB first or LSB first. The default for the AD9549 is MSB first. The LSB first mode can be set by writing a 1 to Register 0000[6] and requires that an I/O update be executed. Immediately after the LSB first bit is set, all serial control port operations are changed to LSB first order.

When MSB first mode is active, the instruction and data bytes must be written from MSB to LSB. Multibyte data transfers in MSB first format start with an instruction byte that includes the register address of the most significant data byte. Subsequent data bytes must follow in order from high address to low address. In MSB first mode, the serial control port internal address generator decrements for each data byte of the multibyte transfer cycle.

When LSB First = 1 (LSB first), the instruction and data bytes must be written from LSB to MSB. Multibyte data transfers in LSB first format start with an instruction byte that includes the register address of the least significant data byte followed by multiple data bytes. The serial control port internal byte address generator increments for each byte of the multibyte transfer cycle.

The AD9549 serial control port register address decrements from the register address just written toward 0000h for multibyte I/O operations if the MSB first mode is active (default). If the LSB first mode is active, the serial control port register address increments from the address just written toward 0x1FFF for multibyte I/O operations.

Unused addresses are not skipped during multibyte I/O operations. The user should write the default value to a reserved register and should only write zeros to unmapped registers. Note that it is more efficient to issue a new write command than to write the default value to more than two consecutive reserved (or unmapped) registers.

Table 10. Serial Control Port, 16-Bit Instruction Word, MSB First

MSB															LSB
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
R/$\overline{W}$	W1	W0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

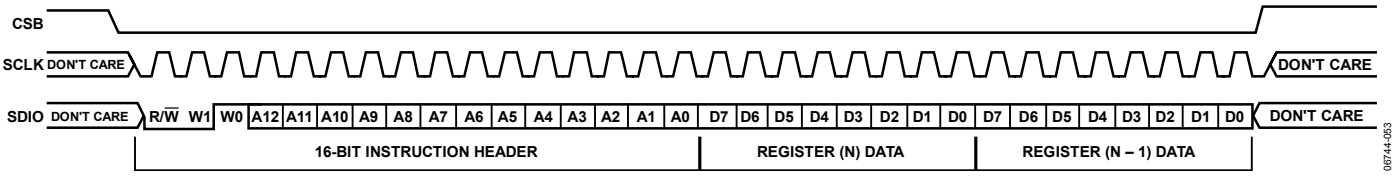


Figure 53. Serial Control Port Write—MSB First, 16-Bit Instruction, 2 Bytes Data

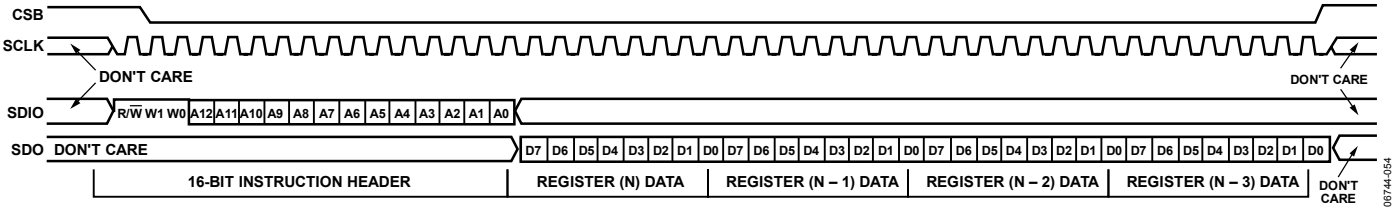


Figure 54. Serial Control Port Read—MSB First, 16-Bit Instruction, 4 Bytes Data

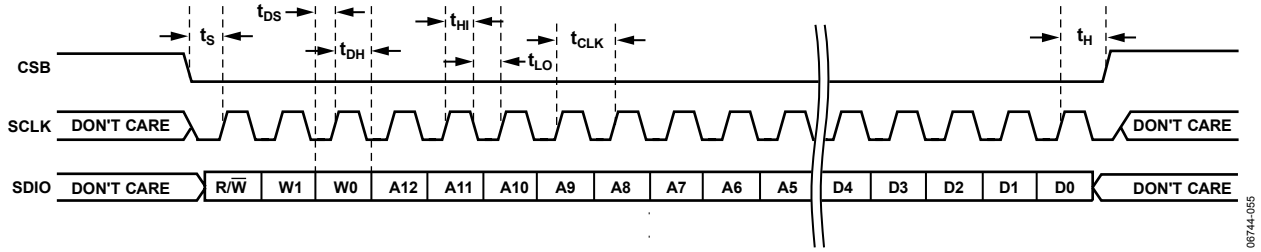


Figure 55. Serial Control Port Write: MSB First, 16-Bit Instruction, Timing Measurements

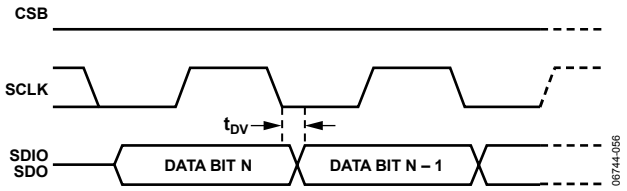


Figure 56. Timing Diagram for Serial Control Port Register Read

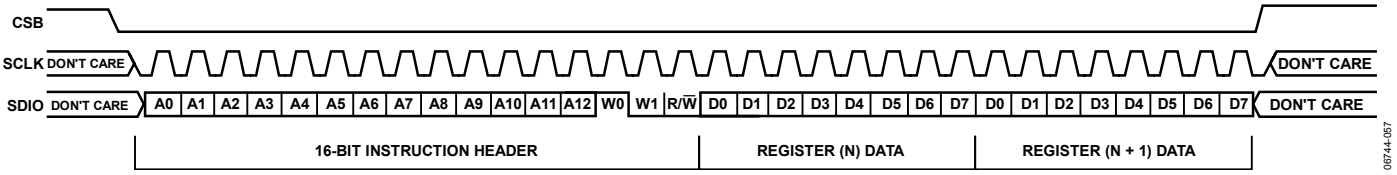


Figure 57. Serial Control Port Write—LSB First, 16-Bit Instruction, 2 Bytes Data

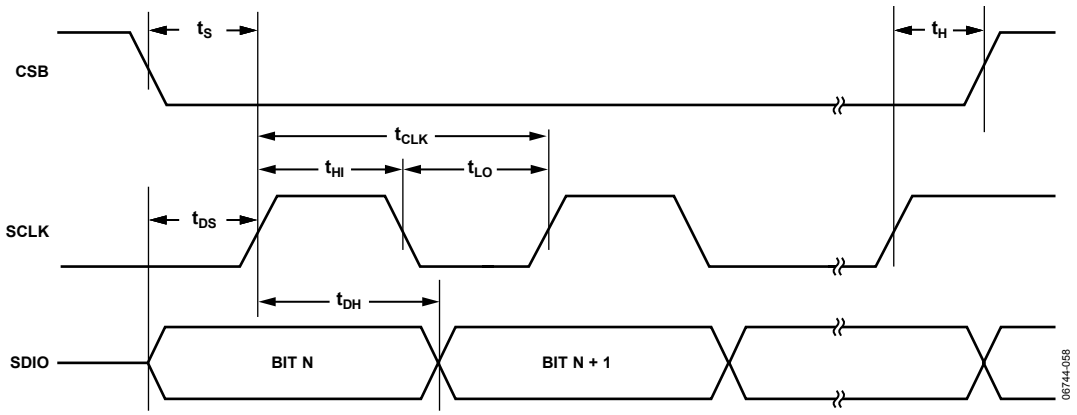


Figure 58. Serial Control Port Timing—Write

Table 11. Definitions of Terms Used in Serial Control Port Timing Diagrams

Parameter	Description
t_{CLK}	Period of SCLK
t_{DV}	Read data valid time (time from falling edge of SCLK to valid data on SDIO/SDO)
t_{DS}	Setup time between data and rising edge of SCLK
t_{DH}	Hold time between data and rising edge of SCLK
t_S	Setup time between CSB and SCLK
t_H	Hold time between CSB and SCLK
t_{HI}	Minimum period that SCLK should be in a logic high state
t_{LO}	Minimum period that SCLK should be in a logic low state

I/O REGISTER MAP

Table 12.

Addr (Hex)	Type[1]	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Serial Port Configuration and Part Identification											
0000		Serial Config.	SDO Active	LSB First (buffered)	Soft Reset	Long Inst.					18
0001		Reserved									00
0002	RO	Part ID	Part ID								02
0003	RO										09
0004		Serial Options								Read Buffer Reg.	00
0005	AC									Register Update	00
Power-Down and Reset											
0010		Power-Down and Enable	PD HSTL Driver	Enable CMOS Driver	Enable Output Doubler	PD SYSCLK PLL	PD REFA	PD REFB	Full PD	Digital PD	00
0011		Reserved									00
0012	M, AC	Reset	History Reset		IRQ Reset	FPFD Reset	CPFD Reset	LF Reset	CCI Reset	DDS Reset	00
0013	M		PD Fund DDS				S Div2 Reset	R Div2 Reset	S Divider Reset	R Divider Reset	00
System Clock											
0020		N-Divider				N-Divider [4:0]					12
0021		Reserved									00
0022		PLL Parameters	VCO Auto Range				2× Refer-ence	VCO Range	Charge Pump Current [1:0]		04
0023		PFD Divider					PFD Divider [3:0] (relationship between SYSCLK and PFD clock)				05
DPLL											
0100	M	PLL Control			Single Tone Mode	Disable Freq. Estimator	Enable Freq. Slew Limiter		Loop Polarity	Close Loop	30
0101		R-Divider	R-Divider [15:0]								00
0102											00
0103			Falling Edge Triggered							R-Divider/2	00
0104		S-Divider	S-Divider [15:0]								00
0105											00
0106			Falling Edge Triggered							S-Divider/2	00
0107	M	P-Divider				P-Divider[4:0]					05

Addr (Hex)	Type[1]	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
0108	M	Loop Coeffi-cients	Alpha-0 [7:0]								00
0109	M						Alpha-0 [11:8]				00
010A	M					Alpha-1 [4:0]					00
010B	M							Alpha-2 [2:0]			00
010C	M		Beta-0 [7:0]								00
010D	M						Beta-0 [11:8]				00
010E	M							Beta-1 [2:0]			00
010F	M		Gamma-0 [7:0]								00
0110	M						Gamma-0 [11:8]				00
0111	M							Gamma-1 [2:0]			00
0112											00
0113											00
0114											00
0115	RO	FTW Estimate	FTW Estimate [47:0] (read-only)								N/A
0116	RO										N/A
0117	RO										N/A
0118	RO										N/A
0119	RO										N/A
011A	RO										N/A
011B	M	FTW Limits	FTW Lower Limit [47:0]								00
011C	M										00
011D	M										00
011E	M										00
011F	M										00
0120	M										00
0121	M		FTW Upper Limit [47:0]								FF
0122	M										FF
0123	M										FF
0124	M										FF
0125	M										FF
0126	M										7F
0127	M	Slew Limit	Frequency Slew Limit [47:0]								00
0128	M										00
0129	M										00
012A	M										00
012B	M										00
012C	M										00
012D		Reserved									00
012E											00
012F											00
0130											00
Free-Run Mode											
01A0		Reserved									00
01A1											00
01A2											00
01A3											00
01A4											00
01A5											00

Addr (Hex)	Type[1]	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
01A6	M	FTW0 (Open-Loop Frequency Tuning Word)	FTW0 [47:0]								00
01A7	M										00
01A8	M										00
01A9	M										00
01AA	M										Startup cond.
01AB	M										Startup cond.
01AC to 01AD	M	Phase (Open Loop Only)	DDS Phase Word [15:0]								00
Reference Selector/Holdover											
01C0	M	Automatic Control				Holdover Mode		Automatic Selector	Automatic Recover	Automatic Holdover	00
01C1	M	Override				Enable Line Card Mode	Enable Ref Input Override	REF_AB	Enable Holdover Override	Holdover On/Off	00
01C2		Averaging Window					FTW Windowed Average Size [3:0]				00
01C3		Reference Validation				Validation Timer [4:0]					00
Doubler and Output Drivers											
0200		HSTL Driver				OPOL (polarity)			HSTL Output Doubler [1:0]		05
0201		CMOS Driver								CMOS MUX	00
Monitor											
0300	RO	Status		PFD Freq Too High	PFD Freq Too Low	Freq. Est. Done	Ref Selected	Free Run	Ph. Lock Detected	Freq. Lock Detected	N/A
0301	RO			REFA Valid	REFA LOR	REFA OOL		REFB Valid	REFB LOR	REFB OOL	N/A
0302	RO	IRQ Status		PFD Freq. Too High	PFD Freq. Too Low	Freq. Est. Done	Ref. Selected	Free Run	Phase Lock Detected	Freq. Lock Detected	00
0303	RO			REFA Valid	REFA LOR	REFA OOL		REFB Valid	REFB LOR	REFB OOL	00
0304		IRQ Mask						Ref. Changed	Leave Free Run	Enter Free Run	00
0305						Freq. Est. Done	Phase Unlock	Phase Lock	Freq. Unlock	Freq. Lock	00
0306					REFA Valid	!REFA Valid	REFA LOR	!REFA LOR	REFA OOL	!REFA OOL	00
0307					REFB Valid	!REFB Valid	REFB LOR	!REFB LOR	REFB OOL	!REFB OOL	00
0308		S1 Pin Config	REF?	REF? LOR	REF? OOL	REF? Not Valid	Phase Lock	Freq. Lock		IRQ	60
0309		S2 Pin Config	REF?	REF? LOR	REF? OOL	REF? Not Valid	Phase Lock	Freq. Lock		IRQ	E0
030A		S3 Pin Config	REF?	REF? LOR	REF? OOL	REF? Not Valid	Phase Lock	Freq. Lock		IRQ	08
030B		S4 Pin Config	REF?	REF? LOR	REF? OOL	REF? Not Valid	Phase Lock	Freq. Lock		IRQ	01

Addr (Hex)	Type[1]	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
030C		Control	Enable REFA LOR	Enable REFA OOL	Enable REFB LOR	Enable REFB OOL			Enable Phase Lock Det.	Enable Freq. Lock Detector	A2
030E	RO	HFTW	Average or Instantaneous FTW [47:0] (read-only) (An I/O update is required to refresh these registers.)								N/A
030F	RO										N/A
0310	RO										N/A
0311	RO										N/A
0312	RO										N/A
0313	RO										N/A
0314	M	Phase Lock	Phase Lock Threshold [31:0]								FF
0315	M										00
0316	M										00
0317	M										00
0318	M		Phase Unlock Watchdog Timer [2:0]			Phase Lock Watchdog Timer [4:0]					FF
0319	M	Frequency Lock	Frequency Lock Threshold [31:0]								00
031A	M										00
031B	M										00
031C	M										00
031D	M		Frequency Unlock Watchdog Timer [2:0]			Frequency Lock Watchdog Timer [4:0]					FF
031E	M	Loss of Reference	REFA LOR Divider [15:0]								FF
031F	M										FF
0320	M		REFB LOR Divider [15:0]								FF
0321	M										FF
0322	M	Reference Out Of Limits	REFA OOL Divider [15:0]								00
0323	M										00
0324	M		REFA OOL Upper Limit [31:0]								FF
0325	M										FF
0326	M										FF
0327	M										FF
0328	M		REFA OOL Lower Limit [31:0]								00
0329	M										00
032A	M										00
032B	M										00
032C	M		REFB OOL Divider [15:0]								00
032D	M										00
032E	M		REFB OOL Upper Limit [31:0]								FF
032F	M										FF
0330	M										FF
0331	M										FF
0332	M		REFB OOL Lower Limit [31:0]								00
0333	M										00
0334	M										00
0335	M										00

Addr (Hex)	Type[1]	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Calibration (User-Accessible Trim)											
0400		K-Divider	K-Divider [15:0]								00
0401											00
0402	M	CPFD Gain						CPFD Gain Scale [2:0]			00
0403	M				CPFD Gain [5:0]						20
0404		FPFD Gain	FPFD Gain [7:0]								C8
0405		Reserved									00
0406											00
0407											00
0408											00
0409	M	PFD Offset	DPLL Phase Offset [7:0]								00
040A	M				DPLL Phase Offset [13:8]						00
040B		DAC Full-Scale Current	DAC Full-Scale Current [7:0]								FF
040C									DAC Full-Scale Current [9:8]		01
040D		Reserved									00
040E		Reserved									10
040F		Reference Bias Level							DC Input Level [1:0]		00
0410		Reserved									00
Harmonic Spur Reduction											
0500	M	Spur A	HSR-A Enable	Amplitude Gain × 2			Spur A Harmonic [3:0]				00
0501	M		Spur A Magnitude [7:0]								00
0502	M										00
0503	M		Spur A Phase [7:0]								00
0504	M									Spur A Phase [8]	00
0505	M	Spur B	HSR-B Enable	Amplitude Gain × 2			Spur B Harmonic [3:0]				00
0506	M		Spur B Magnitude [7:0]								00
0507	M										00
0508	M		Spur B Phase [7:0]								00
0509	M									Spur B Phase [8]	00

[1] Types of registers: M = mirrored (also called buffered). This type of register needs an I/O update for the new value to take effect; RO = read-only; AC = auto-clear.

I/O REGISTER DESCRIPTION

SERIAL PORT CONFIGURATION (REG 0000 TO REG 0005)

Register 0000—Serial Configuration

Table 13.

Bits	Bit Name	Description
D4:D7		These bits are the mirror image of Bits [D0:D3].
D0	SDO Active	Enables SDO Pin. 1 = SDO pin enabled (4-wire serial port mode). 0 = 3-wire mode.
D1	LSB First	Sets bit order for serial port. 1 = LSB first. 0 = MSB first. I/O update must occur in order to take effect.
D2	Soft Reset	Resets register map, except for Register 0000. Setting this bit forces a soft reset, meaning that S1 to S4 are not tri-stated, nor is their state read when this bit is cleared. The AD9549 assumes the values of S1 to S4 that were present during the last hard reset. This bit is not self-clearing, and all other registers are restored to their default values after a soft reset.
D3	Long Instruction	Read-only: this part only supports long instructions.

Register 0001—Reserved

Register 0002 to Register 0003—Part ID (Read-Only)

Register 0004—Serial Options

Table 14.

Bits	Bit Name	Description
D0	Read Buffer Register	For buffered registers, serial port read-back reads from actual (active) registers instead of the buffer. 1 = reads the buffered values that take effect during the next I/O update. 0 = reads values that are currently in effect.

Register 0005—Serial Options (Self Clearing)

Table 15.

Bits	Bit Name	Description
D0	Register Update	Software access to the register update pin function. Writing a 1 to this bit is identical to performing an I/O update.

POWER-DOWN AND RESET (REG 0010 TO REG 0013)

Register 0010—Power-Down and Enable

Power-up default is defined by startup pins.

Table 16.

Bits	Bit Name	Description
D0	Digital PD	Remove clock from most of digital section; leave serial port usable. In contrast to full PD, setting this bit does not debias inputs, allowing for quick wake-up.
D1	Full PD	Setting this bit is identical to activating the PD pin and puts all blocks (except serial port) into power-down mode. SYSCLK is turned off.
D2	PD REFB	Power-down reference clock B input (and related circuits).
D3	PD REFA	Power-down reference clock A input (and related circuits).
D4	PD SYSCLK PLL	System clock multiplier power-down. 1 = system clock multiplier powered down.
D5	Enable Output Doubler	Power up output clock generator doubler. Output doubler must still be enabled in Register 0200.
D6	Enable CMOS Driver	Power up CMOS output driver. 1 = CMOS driver on.
D7	PD HSTL Driver	Power down HSTL output driver. 1 = HSTL driver powered down.

Register 0011—Reserved

Register 0012—Reset (Auto-Clear)

To reset the entire chip, the user can also use the (non-self clearing) Soft Reset bit in Register 0000. Except for IRQ reset, the user normally would not need to use these. However, if the user attempts to lock the loop for the first time when no signal is present, the user should write a 1 to Bits [0:4] of this register before attempting to lock the loop again.

Table 17.

Bits	Bit Name	Description
D0	DDS Reset	Direct digital synthesis reset.
D1	CCI Reset	Cascaded comb integrator reset.
D2	LF Reset	Loop filter reset.
D3	CPFD Reset	Coarse phase frequency detector reset.
D4	FPFD Reset	Fine phase frequency detector reset.
D5	IRQ Reset	Clear IRQ signal and IRQ status monitor.
D6	Reserved	
D7	History Reset	Setting this bit clears the FTW monitor and pipeline.

Register 0013—Reset (Continued) (Not Auto-Clear)

Table 18.

Bits	Bit Name	Description
D0	R Divider Reset	Synchronous (to R-divider prescaler output) reset for integer divider.
D1	S Divider Reset	Synchronous (to S-divider prescaler output) reset for integer divider.
D2	R Div2 Reset	Asynchronous reset for R prescaler.
D3	S Div2 Reset	Asynchronous reset for S prescaler.
D7	PD Fund DDS	Setting this bit powers down the DDS fundamental output but not the spurs. It is used during tuning of the spur killer circuit.

SYSTEM CLOCK (REG 0020 TO REG 0023)

Register 0020—N-Divider

Table 19.

Bits	Bit Name	Description
D4:D0	N-Divider	These bits set the feedback divider for system clock PLL. There is a fixed/2 preceding this block, as well as an offset of 2 added to this value. Therefore, setting this register to 00000 translates to an overall feedback divider ratio of 4. See Figure 43.

Register 0021—Reserved

Register 0022—PLL Parameters

Table 20.

Bits	Bit Name	Description
D1:D0	Charge Pump Current	Charge pump current. 00 = 250 µA. 01 = 375 µA. 10 = off. 11= 125 µA.
D2	VCO Range	Select low range or high range VCO. 0 = low range (700 MHz to 810 MHz). 1 = high range (900 MHz to 1000 MHz). For System clock settings between 810 MHz and 900 MHz, use the VCO Auto Range (Bit 7) to set the correct VCO range automatically.
D2	2× Reference	Enables a frequency doubler prior to the SYSCLK PLL and can be useful in reducing jitter induced by the SYSCLK PLL. See Figure 42.
D4:D6	Reserved	
D7	VCO Auto Range	Automatic VCO range selection. Enabling this bit allows Bit 2 of this register to be set automatically.

Register 0023—PFD Divider

Table 21.

Bits	Bit Name	Description
D3:D0	PFD Divider	Divide ratio for PFD clock from system clock. This is typically varied only in cases where the designer wishes to run the DPLL phase detector fast while SYSCLK is run relatively slowly. The ratio is equal to PFD Divider × 4. For a 1 GHz system clock, the ADC runs at 1 GHz/20 = 50 MHz, and the DPLL phase detector runs at half this speed, which in this case is 25 MHz.

DIGITAL PLL CONTROL AND DIVIDERS (REG 0100 TO REG 0130)

Register 0100—PLL Control

Table 22.

Bits	Bit Name	Description
D0	Close Loop	Setting this bit closes the loop. If Bit 4 of this register is cleared, then the frequency estimator is used. If this bit is cleared and the loop is opened, the user should reset the CCI and LF bits of Register 0012 before closing the loop again.
D1	Loop Polarity	This bit reverses the polarity of the loop response.
D2	Reserved	
D3	Enable Frequency Slew Limiter	This bit enables the frequency slew limiter that controls how fast the tuning word can change and is useful for avoiding runt and stretched pulses during clock switchover and holdover transitions. These values are set in Register 0127 to Register 012C. See the Frequency Slew Limiter section.
D4	Disable Frequency Estimator	The frequency estimator is normally not used but is useful when the input frequency is unknown or needs to be qualified. This estimate appears in Register 0115 to Register 011A. The frequency estimator is not needed when FTW0 (Register 01A6 to Register 01AB) is programmed. See the Frequency Estimator section.
D5	Single Tone Mode	Setting this bit allows the AD9549 to output a tone open loop using FTW0 as DDS tuning word. This bit must be cleared when Bit 0 (Close Loop) is set. This is very useful in debugging when the signal coming into the AD9549 is questionable or nonexistent.
D7:D6	Reserved	

Register 0101 to Register 0102—R-Divider (DPLL Feedforward Divider)

Table 23.

Bits	Bit Name	Description
D15:D0	R-Divider	Feedforward divider (also called the reference divider) of the DPLL. Divide ratio = 1 – 65,536. See the Feedforward Divider (Divide-by-R) section. If the desired feedforward ratio is greater than 65,536, or if the reference input signal on REFA or REFB is greater than 400 MHz, then Bit 0, Register 0103 must be set. Note that the actual R-divider is the value in this register plus one, so to have an R-divider of one, Register 0101 and Register 0102 must both be 0x00. Register 0101 is the least significant byte.

Register 0103—R-Divider (Continued)

Table 24.

Bits	Bit Name	Description
D0	R-Divider/2	Setting this bit enables an additional /2 prescaler, effectively doubling the range of the feedforward divider. If the desired feedforward ratio is greater than 65,536, or if the reference input signal on REFA or REFB is greater than 400 MHz, then this bit must be set.
D6:D1	Reserved	
D7	Falling Edge Triggered	Setting this bit inverts the reference clock before R-divider.

Register 0104 to Register 0105—S-Divider (DPLL Feedback Divider)

Table 25.

Bits	Bit Name	Description
D15:D0	S-Divider	Feedback divider. Divide ratio = 1 – 65,536. If the desired feedback ratio is greater than 65,536, or if the feedback signal on FDBK_IN is greater than 400 MHz, then Bit 0, Register 0106 must be set. Note that the actual S-divider is the value in this register plus one, so to have an R-divider of one, Register 0104 and Register 0105 must both be 0x00. Register 104 is the least significant byte.

Register 0106—S-Divider (Continued)

Table 26.

Bits	Bit Name	Description
D0	S-Divider/2	Setting this bit enables an additional /2 prescaler. See the Feedback Divider (Divide-by-S) section. If the desired feedback ratio is greater than 65,536, or if the feedback signal on FDBK_IN is greater than 400 MHz, then this bit must be set. An example of this case is when the PLL is locking to an image of the DAC output that is above the Nyquist frequency.
D6:D1	Reserved	
D7	Falling Edge Triggered	Setting this bit inverts the reference clock before S-divider.

Register 0107—P-Divider

Table 27.

Bits	Bit Name	Description
D4:D0	P-Divider	Divide ratio. Controls the ratio of DAC sample rate to loop filter sample rate. See the Digital Loop Filter section. Loop filter sample rate = DAC sample rate/2^(divide ratio [4:0]). For the default case of 1 GHz DAC sample rate, and P-Divider [4:0] of 5, the loop filter sample rate is 31.25 MHz. Note that the DAC sample rate is the same as system clock.

Register 0108 to Register 0109—Loop Coefficients

See the Digital Loop Filter Coefficients section. Note that the AD9549 evaluation software will derive these values.

Table 28.

Bits	Bit Name	Description
D11:D0	Alpha-0	Linear coefficient for alpha coefficient.

Register 010A—Loop Coefficients (Continued)

Table 29.

Bits	Bit Name	Description
D4:D0	Alpha-1	Power-of-2 multiplier for alpha coefficient.

Register 010B—Loop Coefficients (Continued)

Table 30.

Bits	Bit Name	Description
D2:D0	Alpha-2	Power-of-2 divider for alpha coefficient.

Register 010C to Register 010D—Loop Coefficients (Continued)

Table 31.

Bits	Bit Name	Description
D11:D0	Beta-0	Linear coefficient for beta coefficient.

Register 010E—Loop Coefficients (Continued)

Table 32.

Bits	Bit Name	Description
D2:D0	Beta-1	Power-of-2 divider for beta coefficient.

Register 010F to Register 0110—Loop Coefficients (Continued)

Table 33.

Bits	Bit Name	Description
D11:D0	Gamma-0	Linear coefficient for gamma coefficient.

Register 0111—Loop Coefficients (Continued)

Table 34.

Bits	Bit Name	Description
D2:D0	Gamma-1	Power-of-2 divider for gamma coefficient.

Register 0112 to Register 0114—Reserved

Register 0115 to Register 011A—FTW Estimate (Read-Only)

Table 35.

Bits	Bit Name	Description
D47:D0	FTW Estimate	This frequency estimate is from the frequency estimator circuit and is informational only. It is useful for verifying the input reference frequency. See the Frequency Estimator section for a description.

Register 011B to Register 0120—FTW Lower Limit

Table 36.

Bits	Bit Name	Description
D47:D0	FTW Lower Limit	Lowest DDS tuning word in closed-loop mode. This feature is recommended when a band-pass reconstruction filter is used. See the Output Frequency Range Control section.

Register 0121 to Register 0126—FTW Upper Limit

Table 37.

Bits	Bit Name	Description
D47:D0	FTW Upper Limit	Highest DDS tuning word in closed- loop mode. This feature is recommended when a band-pass reconstruction filter is used. See the Output Frequency Range Control section.

Register 0127 to Register 012C—Frequency Slew Limit

Table 38.

Bits	Bit Name	Description
D47:D0	Frequency Slew Limit	See the Frequency Slew Limiter section.

Register 012D to Register 0130—Reserved

FREE-RUN (SINGLE-TONE) MODE (REG 01A0 TO REG 01AD)

Register 01A0 to Register 01A5—Reserved

Register 01A6 to Register 01AB—FTW0

Table 39.

Bits	Bit Name	Description
D47:D0	FTW0	FTW (frequency tuning word) for DDS when loop is not closed (see Register 0100, Bit 0). Also used as the initial frequency estimate when the estimator is disabled (see Register 0100, Bit 4) Note that the power-up default is defined by startup Pin S1 to Pin S4. See the Default DDS Output Frequency on Power-Up section.

Register 01AC to Register 01AD—Phase

Table 40.

Bits	Bit Name	Description
D15:D0	DDS Phase Word	Allows user to vary the phase of the DDS output. Active only when loop is not closed.

REFERENCE SELECTOR/HOLDOVER (REG 01C0 TO REG 01C3)

Register 01C0—Automatic Control

Table 41.

Bits	Bit Name	Description
D0	Automatic Holdover	Setting this bit permits state machine to enter holdover (free-run) mode.
D1	Automatic Recover	Setting this bit permits state machine to leave holdover mode.
D2	Automatic Selector	Setting this bit permits state machine to switch the active reference clock input.
D3	Reserved	
D4	Holdover Mode	This bit determines which frequency tuning word (FTW) is used in holdover mode. 0 = use last FTW at time of holdover. 1 = use averaged FTW at time of holdover, which is the recommended setting. The number of averages used is set in Register 01C2.

Register 01C1—Override

Table 42.

Bits	Bit Name	Description
D0	Holdover On/Off	This bit controls the status of holdover when Bit 1 of this register is set.
D1	Enable Holdover Override	Setting this bit disables automatic holdover and allows user to enter/exit holdover manually via Bit 0 (see Bit 0 description). Setting this bit overrides the HOLDOVER pin.
D2	REF_AB	This bit selects the input when Bit 3 of this register is set. 0 = REFA.
D3	Enable Ref Input Override	Setting this bit disables automatic reference switchover, and allows user to switch references manually via Bit 2 of this register. Setting this bit overrides the REFSELECT pin.
D4	Enable Line Card Mode	Enables line card mode of reference switch MUX, which eliminates the possibility of a runt pulse during switchover. See the Use of Line Card Mode to Eliminate Runt Pulses section.

Register 01C2—Averaging Window

Table 43.

Bits	Bit Name	Description
D3:D0	FTW Windowed Average Size	This register sets the number of FTWs (frequency tuning words) that are used for calculating the average FTW. Bit 4 in Register 01C0 enables this feature. An average size of at least 32,000 is recommended for most applications. The number of averages equals $2^{(\text{FTW Windowed Average Size [3:0]})}$. These samples are taken at the rate of ($fs/2^{PIO}$).

Register 01C3—Reference Validation

Table 44.

Bits	Bit Name	Description
D4:D0	Validation Timer	The value in this register sets the time required to validate a reference after an LOR or OOL event before the reference can be used as the DPLL reference. This circuit uses the digital loop filter clock (see Register 0107). Validation time = loop filter clock period × $2^{(\text{Validation Timer [4:0] +1})} - 1$. Assuming power-on defaults, the recovery time varies from 32 ns (00000) to 137 sec (11111). If longer validation times are required, the user can make the P-divider larger. The user should be careful to set the validation timer to at least two periods of the OOL evaluation period. The OOL evaluation period is the period of reference input clock times the OOL divider (Register 0322 to Register 0323).
D7:D5	Reserved	

DOUBLER AND OUTPUT DRIVERS (REG 0200 TO REG 0201)

Register 0200—HSTL Driver

Table 45.

Bits	Bit Name	Description
D1:D0	HSTL Output Doubler	HSTL output doubler. 01 = doubler disabled. 10 = doubler enabled. When using doubler, Register 0010[5] must also be set.
D3:D2	Reserved	
D4	OPOL	Output polarity. Setting this bit inverts the HSTL driver output polarity.

Register 0201—CMOS Driver

Table 46.

Bits	Bit Name	Description
D0	CMOS Mux	User mux control. This bit allows the user to select whether the CMOS driver output is divided by the S-divider. 0 = S-divider input sent to CMOS driver. 1 = S-divider output sent to CMOS driver. See Figure 22.

MONITOR (REG 0300 TO REG 0335)

Register 0300—Status

This register contains the status of the chip. This register is read-only and live update.

Table 47.

Bits	Bit Name	Description
D0	Frequency Lock Detect	This flag indicates that the frequency lock detect circuit has detected frequency lock. This feature compares the absolute value of the difference of two consecutive phase detector edges against a programmable threshold. Because of this, frequency lock detect is more rigorous than phase lock detect, and it is possible to have phase lock detect without frequency lock detect.
D1	Phase Lock Detect	This flag indicates that the phase lock detect circuit has detected phase lock. The amount of phase adjustment is compared against a programmable threshold. Note that this bit can be set in single tone and holdover modes and should be ignored in these cases.
D2	Free Run	DPLL is in holdover mode (free-run).
D3	Reference Selected	Reference selected. 0 = Reference A is active. 1 = Reference B is active.
D4	Frequency Estimator Done	True when the frequency estimator circuit has successfully estimated the input frequency. See the Frequency Estimator section.
D5	PFD Frequency Too Low	This flag indicates that the frequency estimator failed and detected too low of a PFD frequency. This bit is only relevant if the user is relying on the frequency estimator to determine the input frequency.
D6	PFD Frequency Too High	This flag indicates that the frequency estimator failed and detected too high of a PFD frequency. This bit is only relevant if the user is relying on the frequency estimator to determine the input frequency.
D7	Reserved	

Register 0301—Status (Continued)

This register contains the status of the chip. This register is read-only and live update.

Table 48.

Bits	Bit Name	Description
D0	REFB OOL	The OOL (out of limits) circuit has determined that Reference B is out of limits.
D1	REFB LOR	A LOR (loss of reference) has occurred on Reference B.
D2	REFB Valid	The reference validation circuit has successfully determined that Reference B is valid.
D3	Reserved	
D4	REFA OOL	The OOL (out of limits) circuit has determined that Reference A is out of limits.
D5	REFA LOR	A LOR (loss of reference) has occurred on Reference A.
D6	REFA Valid	The reference validation circuit has successfully determined that Reference A is valid.
D7	Reserved	

Register 0302 to Register 0303—IRQ Status

These registers contain the chip status (Registers 0300 to Register 0301) at the time of IRQ. These bits are cleared with an IRQ reset (see Register 0012, Bit 5).

Register 0304—IRQ Mask

Table 49.

Bits	Bit Name	Description
D0	Enter Free Run	Trigger IRQ when DPLL enters free-run (holdover) mode.
D1	Leave Free Run	Trigger IRQ when DPLL leaves free-run (holdover) mode.
D2	Reference Changed	Trigger IRQ when active reference clock selection changes.
D7:D3	Reserved	

Register 0305—IRQ Mask (Continued)

Table 50.

Bits	Bit Name	Description
D0	Frequency Lock	Trigger IRQ on rising edge of frequency lock signal.
D1	Frequency Unlock	Trigger IRQ on falling edge of frequency lock signal.
D2	Phase Lock	Trigger IRQ on rising edge of phase lock signal.
D3	Phase Unlock	Trigger IRQ on falling edge of phase lock signal.
D4	Frequency Estimator Done	Trigger IRQ when the frequency estimator is done.

Register 0306—IRQ Mask (Continued)

Table 51.

Bits	Bit Name	Description
D0	!REFA OOL	Trigger IRQ on falling edge of Reference A's OOL.
D1	REFA OOL	Trigger IRQ on rising edge of Reference A's OOL.
D2	!REFA LOR	Trigger IRQ on falling edge of Reference A's LOR.
D3	REFA LOR	Trigger IRQ on rising edge of Reference A's LOR.
D4	!REFA Valid	Trigger IRQ on falling edge of Reference A's Valid.
D5	REFA Valid	Trigger IRQ on rising edge of Reference A's Valid.
D7:D6	Reserved	

Register 0307—IRQ Mask (Continued)

Table 52.

Bits	Bit Name	Description
D0	!REFB OOL	Trigger IRQ on falling edge of Reference B's OOL.
D1	REFB OOL	Trigger IRQ on rising edge of Reference B's OOL.
D2	!REFB LOR	Trigger IRQ on falling edge of Reference B's LOR.
D3	REFB LOR	Trigger IRQ on rising edge of Reference B's LOR.
D4	!REFB Valid	Trigger IRQ on falling edge of Reference B's Valid.
D5	REFB Valid	Trigger IRQ on rising edge of Reference B's Valid.
D7:D6	Reserved	

Register 0308—S1 Pin Configuration

See the Status and Warnings section. The choice of input for a given pin must be all REFA or all REFB and not a combination of both.

Table 53.

Bits	Bit Name	Description
D0	IRQ	Select IRQ signal for output on this pin.
D1	Reserved	
D2	Frequency Lock	Select frequency lock signal for output on this pin.
D3	Phase Lock	Select phase lock signal for output on this pin.
D4	REF? Not Valid	Select either REFA (0) or REFB (1). Not Valid signal for output on this pin.
D5	REF? OOL	Select either REFA (0) or REFB (1) OOL signal for output on this pin.
D6	REF? LOR	Select either REFA (0) or REFB (1) LOR signal for output on this pin.
D7	REF?	Choose either REFA (0) or REFB (1) for use with Bits [4:6].

Register 0309—S2 Pin Configuration

Same as Register 0308, except applies to Pin S2. See Table 53.

Register 030A—S3 Pin Configuration

Same as Register 0308, except applies to Pin S3. See Table 53.

Register 030B—S4 Pin Configuration

Same as Register 0308, except applies to Pin S4. See Table 53.

Register 030C—Control

Table 54.

Bits	Bit Name	Description
D0	Enable Frequency Lock Detector	Register 0319 must be set up to use this. See the Frequency Lock Detection section.
D1	Enable Phase Lock Detector	Register 0314 to Register 0318 must be set up to use this. See the Phase Lock Detection section.
D3:D2	Reserved	
D4	Enable REFB OOL	The REFB OOL limits are set up in Register 032C to Register 0335.
D5	Enable REFB LOR	The REFB LOR limits are set up in Register 0320 to Register 0321.
D6	Enable REFA OOL	The REFA OOL limits are set up in Register 0322 to Register 032B.
D7	Enable REFA LOR	The REFA LOR limits are set up in Registers 031E to Register 031F.

Register 030D—Reserved

Register 030E to Register 0313—HFTW (Read-Only)

Table 55.

Bits	Bit Name	Description
D47:D0	Average or Instantaneous FTW	These read-only registers are the output of FTW monitor. Average or instantaneous is determined by holdover mode (see Bit 4, Register 01C0). These registers must be manually refreshed by issuing an I/O update.

Register 0314 to Register 0317—Phase Lock

Table 56.

Bits	Bit Name	Description
D31:D0	Phase Lock Threshold	See the Phase Lock Detection section.

Register 0318—Phase Lock (Continued)

Table 57.

Bits	Bit Name	Description
D7:D5	Phase Unlock Watchdog Timer	See the Phase Lock Detection section.
D4:D0	Phase Lock Watchdog Timer	See the Phase Lock Detection section.

Register 0319 to Register 031C—Frequency Lock

Table 58.

Bits	Bit Name	Description
D31:D0	Frequency Lock Threshold	See the Frequency Lock Detection section

Register 031D—Frequency Lock (Continued)

Table 59.

Bits	Bit Name	Description
D7:D5	Frequency Unlock Watchdog Timer	See the Frequency Lock Detection section.
D4:D0	Frequency Lock Watchdog Timer	See the Frequency Lock Detection section.

Register 031E to Register 031F—Loss of Reference

Table 60.

Bits	Bit Name	Description
D15:D0	REFA LOR Divider	See the Loss of Reference section.

Register 0320 to Register 0321—Loss of Reference (Continued)

Table 61.

Bits	Bit Name	Description
D15:D0	REFB LOR Divider	See the Loss of Reference section.

Register 0322 to Register 0323—Reference Out Of Limits (OOL)

Table 62.

Bits	Bit Name	Description
D15:D0	REFA OOL Divider	See the Reference Frequency Monitor section. R0322 is the LSB, and R0323 is the MSB.

Register 0324 to Register 0327—Reference OOL (Continued)

Table 63.

Bits	Bit Name	Description
D31:D0	REFA OOL Upper Limit	See the Reference Frequency Monitor section.

Register 0328 to Register 032B—Reference OOL (Continued)

Table 64.

Bits	Bit Name	Description
D31:D0	REFA OOL Lower Limit	See the Reference Frequency Monitor section.

Register 032C to Register 032D—Reference OOL (Continued)

Table 65.

Bits	Bit Name	Description
D15:D0	REFB OOL Divider	See the Reference Frequency Monitor section. R032C is the LSB, and R032D is the MSB.

Register 032E to 0331—Reference OOL (Continued)

Table 66.

Bits	Bit Name	Description
D31:D0	REFB OOL Upper Limit	See the Reference Frequency Monitor section.

Register 0332 to Register 0335—Reference OOL (Continued)

Table 67.

Bits	Bit Name	Description
D31:D0	REFB OOL Lower Limit	See the Reference Frequency Monitor section.

CALIBRATION (USER-ACCESSIBLE TRIM) (REG 0400 TO REG 0410)

Register 0400 to Register 0401—K-Divider

Table 68.

Bits	Bit Name	Description
D15:D0	K-Divider	The K-divider alters precision of frequency estimator circuit. See the Frequency Estimator section.

Register 0402—CPFD Gain

Table 69.

Bits	Bit Name	Description
D2:D0	CPFD Gain Scale	This register is the coarse phase frequency power-of-2 multiplier (PDS). See the Phase Detector section. Note that the correct value for this register will be calculated by filter design software provided with the evaluation board.

Register 0403—CPFD Gain (Continued)

Table 70.

Bits	Bit Name	Description
D5:D0	CPFD Gain	This register is the coarse phase frequency linear multiplier (PDG). See the Phase Detector section. Note that the correct value for this register will be calculated by filter design software provided with the evaluation board.

Register 0404—FPFD Gain

Table 71.

Bits	Bit Name	Description
D7:D0	FPFD Gain	This register is the fine phase frequency detector linear multiplier (alters charge pump current). See the Fine Phase Detector section. Note that the correct value for this register will be calculated by filter design software provided with the evaluation board.

Register 0405 to Register 0408—Reserved

Register 0409 to Register 040A—PFD Offset

Table 72.

Bits	Bit Name	Description
D13:D0	DPLL Phase Offset	This register controls the static time offset of the PFD (phase frequency detector) in closed-loop mode. It has no effect when the DPLL is open.

Register 040B—DAC Full-Scale Current

Table 73.

Bits	Bit Name	Description
D7:D0	DAC Full-Scale Current	DAC Full-Scale Current [7:0]. See the DAC Output section.

Register 040C—DAC Full-Scale Current (Continued)

Table 74.

Bits	Bit Name	Description
D1:D0	DAC Full-Scale Current	DAC Full-Scale Current [9:8]. See Register 040B.

Register 040D to Register 040E—Reserved

Register 040F—Reference Bias Level

Table 75.

Bits	Bit Name	Description
D1:D0	DC Input Level	DC input level for VDDX @ 3.3 V. This register sets the dc bias level for the reference inputs. The value should be chosen such that VIH is as close as possible to (but not exceeding) 3.3 V. 00 = VDD3 – 800 mV. 01 = VDD3 – 400 mV. 10 = VDD3 – 1.6 V. 11 = VDD3 – 1.2 V.
D7:D2	Reserved	

Register 0410—Reserved

HARMONIC SPUR REDUCTION (REG 0500 TO REG 0509)

See the Harmonic Spur Reduction section.

Register 0500—Spur A

Table 76.

Bits	Bit Name	Description
D3:D0	Spur A Harmonic	Spur A Harmonic 1 – 15.
D5:D4	Reserved	
D6	Amplitude Gain × 2	
D7	HSR-A Enable	Harmonic Spur Reduction A enable.

Register 0501 to Register 0502—Spur A (Continued)

Table 77.

Bits	Bit Name	Description
D7:D0	Spur A Magnitude	Linear multiplier for Spur A magnitude.

Register 0503 to Register 0504—Spur A (Continued)

Table 78.

Bits	Bit Name	Description
D8	Spur A Phase	Linear offset for Spur A phase.

Register 0505—Spur B

Table 79.

Bits	Bit Name	Description
D3:D0	Spur B Harmonic	Spur B Harmonic 1 – 15.
D5:D4	Reserved	
D6	Amplitude Gain × 2	
D7	HSR-B Enable	Harmonic Spur Reduction B enable.

Register 0506 to Register 0507—Spur B (Continued)

Table 80.

Bits	Bit Name	Description
D7:D0	Spur B Magnitude	Linear multiplier for Spur B magnitude.

Register 0508 to Register 0509—Spur B (Continued)

Table 81.

Bits	Bit Name	Description
D8	Spur B Phase	Linear offset for Spur B phase.

SAMPLE APPLICATION CIRCUIT

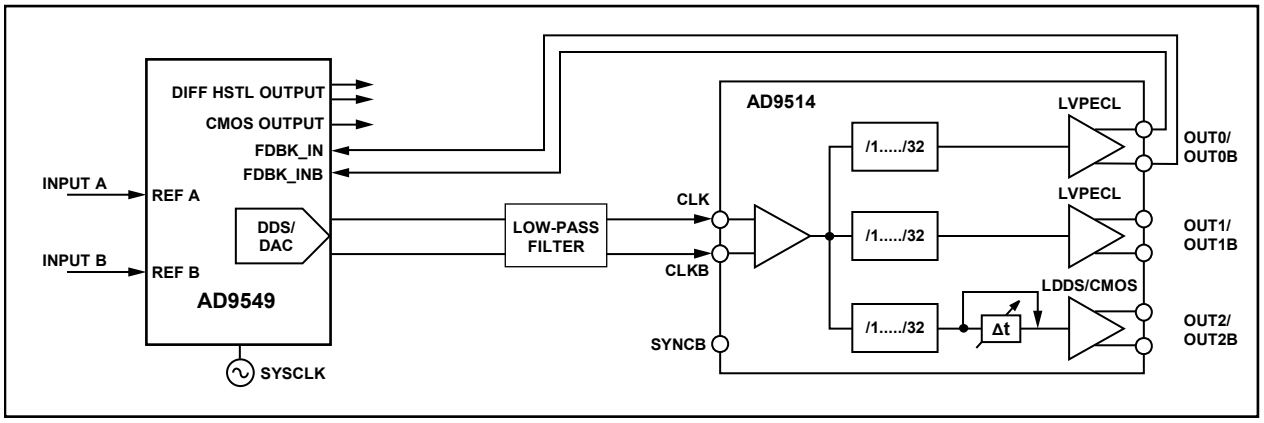


Figure 59. AD9549 and AD9514 Precision Clock Distribution Circuit

Features of this application circuit include:

- Input frequencies down to 8 kHz. Output frequencies up to 400 MHz.
- Programmable loop bandwidth down to < 1 Hz.
- Automatic redundant clock switchover with user-selectable rate of phase adjustment.
- Automatic stratum 3/3E clock holdover, depending on configuration.
- Phase noise (f_C = 122.3 MHz and 100 Hz loop BW): 100 Hz offset: −107 dBc/Hz. 1 kHz offset: −142 dBc/Hz. 100 kHz offset: −157 dBc/Hz. Two zero delay outputs with programmable postdivider and synchronization.
- Two additional outputs (nonzero delay) on AD9549.
- Programmable skew adjustment on one AD9514 output.

OUTLINE DIMENSIONS

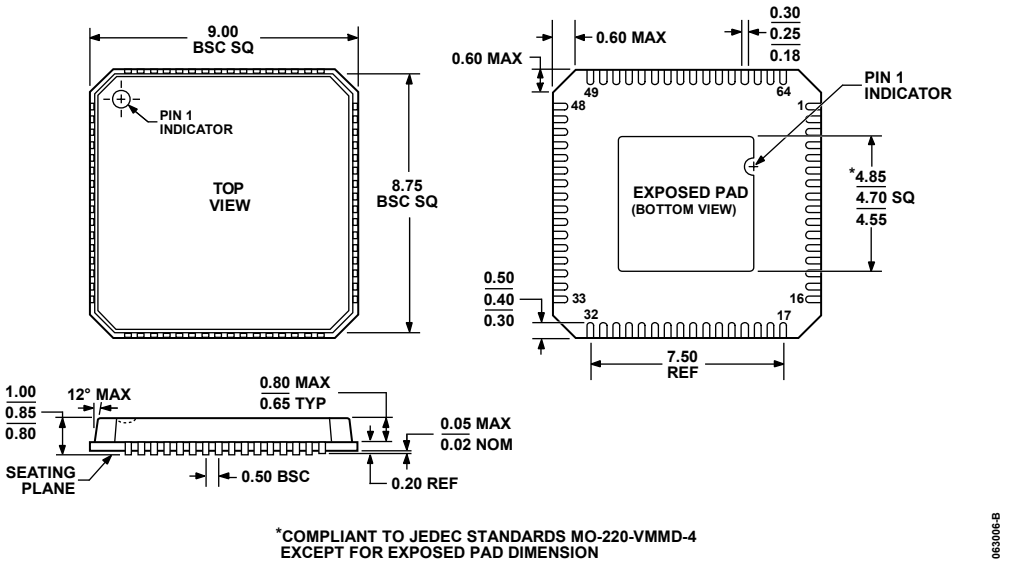


Figure 60. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
9 mm × 9 mm Body, Very Thin Quad
(CP-64-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9549BCPZ[1]	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-1
AD9549BCPZ-REEL7[1]	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-1
AD9549/PCBZ[1]	−40°C to +85°C	Evaluation Board	CP-64-1

[1] Z = RoHS Compliant Part.

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